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(73) Proprietor: **MITSUBISHI DENKI KABUSHIKI KAISHA**
Tokyo 100 (JP)

(72) Inventors:
- **Yamaguchi, Yasuo, Mitsubishi Denki K.K. LSI Itami-shi, Hyogo 664 (JP)**
- **Nishimura, Tadashi, Mitsubishi Denki K.K. LSI Itami-shi, Hyogo 664 (JP)**

(74) Representative:
Beresford, Keith Denis Lewis et al
BERESFORD & Co.
High Holborn
2-5 Warwick Court
London WC1R 5DJ (GB)

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- **PATENT ABSTRACTS OF JAPAN vol. 017, no. 227 (E-1360), 10 May 1993 & JP 04 359470 A (VICTOR CO OF JAPAN LTD), 11 December 1992**

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a semiconductor device including a MOS (Metal Oxide Semiconductor) field effect transistor (hereinafter referred to as "MOSFET") formed on a semiconductor substrate and, more particularly, to an improvement in supplying a substrate bias voltage.

Description of the Background Art

[0002] Generally, a semiconductor device such as a dynamic random access memory and a static random access memory is constituted by a number of MOS transistors formed on one semiconductor substrate. Normally, the potential of the semiconductor substrate is constantly maintained in a predetermined range in such a semiconductor device.

[0003] Fig. 20 is a schematic block diagram of such a semiconductor device. Referring to Fig. 20, the semiconductor device 100 includes functional circuit (or internal circuit) 110 and a substrate bias generating circuit 120 formed on a single semiconductor substrate. The functional circuit 110 is constituted by a number of MOS transistors for implementing functions necessary for the semiconductor device 100. The substrate bias generating circuit 120 is also constituted by MOS transistors and it generates a substrate bias voltage V_{BB} for maintaining the semiconductor substrate 1 at a predetermined negative potential.

[0004] Fig. 21 is a cross sectional view showing a portion of a cross sectional structure of a general integrated circuit device. The functional circuit 110 shown in Fig. 20 includes the sectional structure shown in Fig. 21. Fig. 21 shows, as an example, an NMOS transistor and interconnections provided in the periphery thereof. Referring to Fig. 21, the NMOS transistor includes N type impurity regions 2 and 3 serving as source and drain formed near the main surface of the semiconductor substrate 1 and a gate electrode 5. A gate dielectric thin film 4 is formed between the gate electrode 5 and the substrate 1. P type impurities of low concentration (for example 10^{16} to $10^{17}/cm^3$) are introduced to the silicon substrate 1 below the gate electrode 5. N type impurities of high concentration (for example, 10^{19} to $10^{21}/cm^3$) are introduced to the source region 2 and the drain region 3. Interconnection layers 22 and 23 having low resistance are connected through contact holes formed in an interlayer insulating film 24 to the gate electrode 5, the source region 2 and to the drain region 3.

[0005] In the MOS transistor formed as described above, when a positive voltage is applied to the gate electrode 5, N type carriers (electrons) are induced at an upper layer portion of the silicon substrate 1 of P-region. More specifically, the surface of the silicon substrate 1 is inverted to N type, so that the surface of the silicon substrate 1 has the same type of conductivity as that of the source region 2 and the drain region 3. Thus it becomes possible for a current to flow between the drain region and source region. The concentration of the N-type carriers induced on the surface of the silicon substrate 1 changes dependent on the voltage applied to the gate electrode 5, and therefore the amount of current flowing between the source region 2 and the drain region 3 can be controlled by the gate voltage.

[0006] In operation, when the NMOS transistor is rendered conductive, hot electrons and holes which constitute pairs are generated near the drain region 3. Most of the generated hot electrons flow to the drain region 3. Meanwhile, most of the generated holes flow to the silicon substrate 1. Thus the potential of the silicon substrate 1 rises. The rise of the potential of the silicon substrate 1 causes the following problem.

[0007] Since PN junctions are formed between the P type silicon substrate 1 and the source region 2 and between the substrate 1 and the drain region 3, the PN junctions are brought to the forward bias state. Accordingly, leak current flows between the silicon substrate 1 and the source region 2 and the drain region 3. Consequently, there is a possibility that the channel is not formed between the source region 2 and the drain region 3, or that the signal to be transmitted is delayed.

[0008] In order to prevent the above problem, the substrate bias generating circuit 120 for keeping the potential V_{BB} of the substrate 1 at about -1V, for example, is provided.

[0009] The conventional operation for supplying substrate bias will be described with reference to Fig. 22. Fig. 22 shows the threshold voltages and the drivability of supplying current when the substrate bias potential is set at -1V. Referring to Fig. 22, the solid lines represent the threshold voltage and the drivability of supplying current when the substrate bias potential is at -1V. In the figure, (a) represents the substrate bias potential, (b) represents the threshold voltages of the NMOS transistor and (c) represents the drivability of supplying current of the NMOS transistor.

[0010] A constant substrate bias is applied (in Fig. 22, - 1V) to the silicon substrate 1 no matter whether it is in an active state or in a standby state. The threshold voltage changes in the negative direction when the substrate bias changes in the positive direction. By the change of the threshold voltage, the drivability of supplying current also changes. In the NMOS transistor, when the threshold voltage changes in the negative direction, the drivability of supplying current increases, while in a PMOS transistor, when the threshold voltage changes in the positive direction, the drivability of supplying current increases. However, in the conventional method of supplying the substrate bias, a constant substrate bias is applied, and therefore the threshold voltage and the current supplying drivability do not change

as shown in Fig. 22.

[0011] Since the conventional semiconductor device is structured as described above, when the threshold voltage is set to minimize the leak current in the standby state, the drivability of supplying current at the active state becomes small, which prevents high speed operation.

[0012] Conversely, if the drivability of supplying current is increased and the threshold value is lowered in order to operate the NMOS transistor at high speed, the leak current in the standby state increases.

[0013] Now, Japanese Patent Laying-Open No. 3-29183 discloses a semiconductor memory device in which substrate potential is switched between an active state and a standby state and in which a deeper substrate bias voltage is applied at the standby state than at the active state.

[0014] Fig. 23 is a block diagram showing the device for switching the substrate bias disclosed in the aforementioned article. Referring to Fig. 23, this device includes an identifying circuit 101 for identifying the active mode and the standby mode; a substrate potential generating circuit 102 having large current drivability for generating a second substrate potential at the active state; a substrate potential generating circuit 103 having smaller current drivability for generating a first substrate potential causing deeper reverse bias than the second substrate potential at the standby state; a comparing circuit 104 for comparing the substrate potential and a reference potential corresponding to the second substrate potential; a comparing circuit 105 for comparing the substrate potential with a reference potential corresponding to the first substrate potential; and a control portion 106 for selecting one of the substrate potential generating circuits 102 and 103 in response to an output signal from the identifying circuit 101 and maintaining constant the substrate potential generated by the selected substrate potential generating circuit in response to output signals from the comparing circuits 104 and 105.

[0015] The current drivability of the substrate potential generating circuit 102 is smaller than that of the circuit 103, since, at the standby state, the first substrate potential is generated only to prevent dissipation of the data stored in the memory cell. However, since the current drivability is small, there is a possibility that the PN junction is set to the forward biased state by the external noise. In order to prevent the forward biased state, the first substrate potential is set to a potential providing deep reverse bias.

[0016] In this prior art, the second substrate potential is made to provide shallower bias than the first substrate potential, since at the active state, there is an internal signal (for example, word lines of the memory) which is raised to be higher than the supply voltage and when the same reverse bias as the first substrate potential is applied, there is a possibility that the breakdown voltage of the PN junction is exceeded.

[0017] In operation, when a signal designating the active mode is input externally, identifying circuit 101 recognizes that it is the active mode, and let control portion 106 control in a manner corresponding to the active mode. Control portion 106 controls the substrate potential generating circuit 102 in response to the output from comparing circuit 104 and maintains the voltage of the substrate at the second substrate potential.

[0018] Meanwhile, when a signal designating the standby mode is input externally, identifying circuit 101 recognizes that it is the standby mode, and let the control portion 106 control in the manner corresponding to the standby mode. Control portion 106 controls substrate potential generating circuit 103 in response to the output from comparing circuit 105 and maintains the substrate potential at the first substrate potential. By doing so, the reverse bias at the standby state can be made deeper than the reverse bias at the active state, and therefore dissipation of data stored in the memory cell in the standby state can be prevented.

[0019] Fig. 24 is a graph showing an example of the relation between the supply voltage Vcc and the first and second substrate potentials b and a generated by the device shown in Fig. 23. As is apparent from Fig. 24, when the supply voltage Vcc is at 5V, the first substrate potential b is - 4V and the second substrate potential a is -3V. The voltage (-3V) of the second substrate potential is similar to the substrate potential of the conventional general semiconductor device, and it is determined based on the relation with respect to the impurity concentration doped in the substrate.

[0020] Therefore, the speed of operation of the semiconductor device is approximately the same as that in the conventional general semiconductor device, and therefore, the speed of operation of the transistor can not be expected to be faster in the active state.

[0021] In order to increase the speed of operation of the semiconductor memory device, it is necessary to determine the voltage of the substrate potential taking into consideration the current drivability and the threshold voltage of the MOS transistor internally provided. Further, it is necessary to determine the first substrate potential taking into consideration the relation between the threshold voltage and the current drivability.

[0022] The prior art shown in Fig. 23 is silent about these relations.

SUMMARY OF THE INVENTION

[0023] The present invention was made to solve the above described problem and its object is to provide a semiconductor device in which current consumption in the standby state can be made smaller and the speed of operation in the active state can be increased.

[0024] Briefly stated, the semiconductor device of the present invention is specified by claim 1.

[0025] The semiconductor device according to the present invention includes a buried insulator layer formed on a semiconductor substrate, a semiconductor

layer formed on the buried insulator layer, and a CMOS circuit including MOS transistors of the first and second conductivity types formed on the semiconductor layer. The semiconductor device further includes a first region, a second region, first to fourth bias voltage generating devices and a bias voltage supplying device. The first region is provided in the buried insulator layer below the MOS transistor of the first conductivity type.

[0026] The second region is provided in the buried insulator layer below the MOS transistor of the second conductivity type.

[0027] The first bias voltage generating device generates a first bias voltage for determining the magnitude of leak current in the inactive state of the MOS transistor of the first conductivity type.

[0028] The third bias voltage generating device generates a third bias voltage for minimizing the magnitude of leak current in the inactive state of the MOS transistor of the second conductivity type.

[0029] The second bias voltage generating device generates a second bias voltage for maximizing the drivability of supplying current in the active state of the MOS transistor of the first conductivity type, with the bias made shallower than the first bias voltage.

[0030] The fourth bias voltage generating device generates a fourth bias voltage for maximizing the drivability of supplying current in the active state of the MOS transistor of the second conductivity type, with the bias made shallower than the third bias voltage.

[0031] The bias voltage supplying device supplies, instead of the first bias voltage, the second bias voltage to the first region, and supplies, instead of the third bias voltage, the fourth bias voltage to the second region, in response to a signal for making active the CMOS circuit.

[0032] In this aspect of the present invention, first and second regions are formed in the buried insulator layer in accordance with the third aspect described above, and various voltages are supplied to the first and second regions. By supplying the first bias voltage to the first region and the third bias voltage to the second region, biases of the MOS transistors are made shallower, the magnitude of leak current in the standby state is reduced, and accordingly, power consumption can be reduced. By supplying the second bias voltage to the first region and fourth bias voltage to the second region, the biases of the MOS transistors are made shallower, and accordingly, the speed of operation in the active state can be increased.

[0033] The objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] Fig. 1 is a block diagram showing a semiconductor device useful for understanding the invention.

[0035] Fig. 2 is a cross section of a portion of the semiconductor device shown in Fig. 1.

[0036] Fig. 3 is an illustration showing changes of the threshold voltage and the drivability of supplying current when the substrate bias is switched.

[0037] Fig. 4A is a graph showing relation between substrate bias and power consumption.

[0038] Fig. 4B shows a change in I_D - V_G characteristic incidental to the change in the substrate bias.

[0039] Fig. 5A shows a change in I_D - V_D characteristic incidental to the change in the substrate bias.

[0040] Fig. 5B shows improvement of the speed of operation with respect to the change in the substrate bias.

[0041] Fig. 6 is a schematic diagram showing an example of the first bias generating circuit shown in Fig. 1.

[0042] Fig. 7A is a block diagram showing an example of the second bias generating circuit shown in Fig. 1.

[0043] Fig. 7B is a block diagram showing another example of the second bias generating circuit shown in Fig. 1.

[0044] Fig. 8 is a schematic diagram showing an example of the bias selecting circuit shown in Fig. 1.

[0045] Fig. 9 is a block diagram of another semiconductor device useful for understanding the invention.

[0046] Fig. 10 is a cross section of a portion of the semiconductor device shown in Fig. 9.

[0047] Fig. 11 is a plan view showing a portion of the semiconductor device shown in Fig. 9.

[0048] Fig. 12 shows changes in the substrate bias, the threshold voltage and the drivability of supplying current when the semiconductor device of Fig. 9 is switched from the standby state to the active state.

[0049] Fig. 13 is a schematic diagram showing an example of the bias selecting circuit shown in Fig. 9.

[0050] Fig. 14 is a cross section showing an embodiment of the semiconductor device in accordance with the present invention.

[0051] Fig. 15 shows changes in the substrate bias, the threshold voltage and the drivability of supplying current when the semiconductor device of Fig. 14 is switched from the standby state to the active state.

[0052] Fig. 16 is a cross sectional view showing a further embodiment of the semiconductor device in accordance with the present invention.

[0053] Fig. 17 is a plan view of the semiconductor device shown in Fig. 16.

[0054] Fig. 18 shows changes in the substrate bias, the threshold voltage and the drivability of supplying current when the device is switched from the standby state to the active state.

[0055] Fig. 19 shows a step of forming the SOI structure shown in Fig. 16.

[0056] Fig. 20 is a block diagram showing an example of a conventional semiconductor device.

[0057] Fig. 21 is a cross section of a portion of the semiconductor device shown in Fig. 20.

[0058] Fig. 22 is a diagram showing a method of supplying substrate bias in the semiconductor device

shown in Fig. 20.

[0059] Fig. 23 shows a conventional substrate bias switching device.

[0060] Fig. 24 shows the substrate potential-supply voltage characteristic of the device shown in Fig. 23.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0061] Fig. 1 is a block diagram showing a semiconductor device useful for understanding the invention. Referring to Fig. 1, the semiconductor device 200 includes a functional circuit 110, a first bias generating circuit 30, a second bias generating circuit 31 and a bias selecting circuit 32 formed on a single silicon substrate 1.

[0062] The functional circuit 110 is the same as that shown in Fig. 20. The first bias generating circuit 30 generates a substrate bias VBB1 in the standby state. The substrate bias VBB1 is determined such that the threshold voltage Vth of the NMOS transistor is set to 0.8V. The potential of the substrate bias VBB1 is related with the drivability of supplying current (mutual conductance) of the NMOS transistor. When the gate width W is 10μm and the gate length L is 1μm, VBB1 is about -3V. By supplying such deep reverse bias, leak current in the standby state can be minimized.

[0063] The second bias generating circuit 31 generates a substrate bias VBB2 in the active state. The substrate bias VBB2 is determined based on the drivability of supplying current in the active state of the NMOS transistor. The drivability of supplying current becomes larger as the threshold voltage Vth becomes smaller, and the drain current flows more easily. In other words, by determining the threshold voltage Vth, the power supply voltage Vdd, the gate width and the gate length, the drivability of supplying current is also determined. In this embodiment, the substrate bias VBB2 is 0V and the threshold voltage Vth is 0.2V, and the current supplying drivability is increased by about 30% than the drivability in the standby state.

[0064] The bias selecting circuit 32 is connected to the first and second bias generating circuits 30 and 31 and it selects the substrate bias VBB2 generated by the second bias generating circuit 31 in response to a control signal CNT, and applies this to the silicon substrate 1.

[0065] Fig. 2 is a cross section of a portion of the semiconductor device shown in Fig. 1. The semiconductor device shown in Fig. 2 differs from the semiconductor device of Fig. 21 in that the substrate bias VBB1 or VBB2 is supplied to the rear surface of the silicon substrate 1. The substrate bias VBB1 is -3V, and the source region 2 and the drain region 3 of the silicon substrate 1 are deeply reverse-biased.

[0066] Fig. 3 shows changes in the threshold voltage and the drivability of supplying current when the substrate bias is switched from VBB1 to VBB2. Fig. 4A is a graph showing the relation between the substrate bias and power consumption. Fig. 4B shows changes in the I_D - V_G characteristic incidental to the change of the substrate bias. Fig. 5A shows changes in the I_D - V_D characteristic incidental to the change of the substrate bias.

[0067] Referring to Fig. 4A, the most appropriate voltage of the substrate potential VBB1 in an MOS transistor having the gate width W of 10μm and the gate length L of 1μm will be described. The substrate bias VBB1 is determined mainly based on the relation between the power consumption of the first bias generating circuit 30 itself and the amount of leak current. In Fig. 4A, the dotted line represents power consumption when the substrate bias VBB1 generated by the first bias generating circuit 30 is changed, and one-dotted line represents the magnitude of leak current when the substrate bias VBB1 is changed. The power consumption at the standby state corresponds to the sum (the solid line of Fig. 4A) of the power consumption by the first bias generating circuit 30 itself and the power consumption caused by the leak current.

[0068] Therefore, the most suitable substrate bias is -3V at which the sum of the power consumption becomes minimum.

[0069] Referring to Fig.4B, the solid line shows the I_D - V_G characteristic when the substrate bias is set to VBB1 (=-3V), while the dotted line represents the I_D - V_G characteristic when the substrate bias is set to VBB2 (= 0V). Here, the threshold voltage Vth is defined by the gate voltage when a drain current of 10^{-6}A flows. Since the magnitude of leak current when the gate voltage V_G at the standby state is set to 0V is set to be not higher than 10^{14}A, the threshold voltage Vth when the substrate bias VBB1 (= -3V) is applied to the substrate becomes 0.8V. Therefore, the ratio of the threshold value Vth with respect to the supply voltage Vcc is increased, and the speed of operation is decreased. Therefore, by setting the substrate bias VBB2 at 0V in the active state, the threshold voltage Vth is lowered to 0.2V so as to reduce the ratio of the threshold voltage Vth with respect to the supply voltage Vcc, and thus the speed of operation can be improved. The value of 0V enables increase of drivability of the transistor at the active state.

[0070] When substrate bias VBB1 is supplied, that is, at the standby state, when the gate voltage becomes lower than 0.8V, the drain current reduces exponentially, and when the gate voltage is 0 (off state), the current lowers to the lowest level and the NMOS transistor is at the cut-off state. Therefore, power consumption can be sufficiently reduced at the standby state.

[0071] As the LSI technique has been developed, MOS transistors have been miniaturized, and in a 5V system, the gate length is 0.8μm, and in a 3V system, the gate length is 0.5μm. In a 1.5V system which will be manufactured in the future, the gate length is expected to be 0.15μm. However, the threshold voltage at the standby state is constant because of the transistor characteristic, and therefore in the 1.5V system, even when

Vth can be reduced to 0.5V, the ratio of the threshold voltage Vth with respect to the operating voltage will be as high as 33%. Therefore, the method of reducing the threshold voltage by changing the substrate bias shown in Fig. 4B becomes very effective.

[0072] Referring to Fig. 5A, the solid line represents the I_D - V_D characteristic when the substrate bias VBB (-3V) is supplied, while the dotted line represents the I_D - V_D characteristic when the substrate bias VBB2(0V) is supplied. From this figure, it can be seen that the speed of rise is improved when the substrate bias VBB2 is supplied as shown in Fig. 5B.

[0073] The operation of the semiconductor device shown in Figs. 1 and 2 will be described with reference to Fig. 3.

[0074] In the standby state, since the substrate bias VBB1 is supplied to the silicon substrate 1, the threshold voltage Vth is 0.8V, and the current supplying drivability is 100% as in the conventional example. In this state, the silicon substrate 1, the source region 2 and the drain region 3 are deeply reverse-biased, which can minimize the amount of leak current.

[0075] Then the aforementioned control signal CNT is applied to the bias selecting circuit 32 for switching the NMOS transistor from the standby state to the active state. In response to the control signal CNT, the bias selecting circuit 32 selects the substrate bias VBB2 instead of the substrate bias VBB1. Consequently, the reverse-bias between the silicon substrate 1 and the source region 2, and between the substrate and the drain region 3 becomes shallower, the threshold voltage Vth attains to 0.2V, the current supplying drivability is increased to about 130%, and the resistance between the drain region and the source region is made smaller. When a positive voltage is supplied to the gate electrode 5 in this state, the channel region is quickly inverted to the N type, which increases the speed of operation.

[0076] As the threshold voltage Vth lowers, the amount of current increases as shown in Figs. 3 and 5. Namely, the leak current in the active state is increased to 10^{-9}A (V_G = 0V). However, power consumption in the active state is not determined by the amount of leak current but by the current charging/discharging the capacitors of the circuit. Therefore, the increase in the power consumption is neglectable. Therefore, by changing the substrate bias in the standby state and in the active state, the power consumption in the standby state can be reduced, and the speed operation in the active state can be improved.

[0077] Although an NMOS transistor is used in the embodiment shown in Figs. 1 to 5, the similar operation is done in a PMOS transistor. More specifically, if the substrate bias is reduced from 8V to 5V and the threshold voltage is changed from 4.2V to 4.8V, the drivability of supplying current is improved and the speed of operation is increased. This correspond to an example in which a supply voltage in the rage of 0 to 5V is used. If a supply voltage in the rage of -5 to 0V is used, the change of the substrate bias is 3V to 0V, and the threshold voltage changes from -0.8V to -0.2V. More specifically, in the PMOS transistor, the substrate bias changes in the direction of the drain bias, as viewed from source bias. The change of the threshold voltage is in the direction of the source bias.

[0078] Fig. 6 is a schematic diagram showing the first bias generating circuit shown in Fig. 1. Referring to Fig. 6, the first bias generating circuit 30 includes a ring oscillator 301 and a charge pump circuit 302. The ring oscillator 301 includes a plurality of cascade connected invertors 303, 304 and 305. The ring oscillator 301 oscillates when the output is fed back to the input, and generates a signal of a prescribed frequency. The charge pump circuit 302 includes a driver 306, capacitors 307 and 310, and diodes 308 and 309. The driver 306 amplifies the signal of a prescribed period from the ring oscillator 301 and applies the amplified signal to one end of the capacitor 307. When the output from the driver 306 lowers from the supply potential to the ground potential, the voltage at the other end of the capacitor 307 also lowers. When the diode 309 is turned on, the discharging path of the capacitor 307 is cut off, and because of the negative charges discharged from the capacitor 307, the potential at the other end of the capacitor 307 is further lowered, to finally reach the negative potential (-Vcc) having the same absolute value as the supply potential Vcc. As a result, the diode 308 is turned on, and the substrate bias VBB1 attains -Vcc + Vth, where Vth is the threshold voltage of the diode 308. By providing a plurality of diodes 308, the substrate bias VBB1 is made to have a desired potential (-3V).

[0079] Fig. 7A and Fig. 7B are schematic diagrams showing examples of the second bias generating circuit 31 shown in Fig. 1. Referring to Fig. 7A, the circuit differs from that of Fig. 6 in that a diode 313 is added to the charge pump circuit 312. As described with reference to Fig. 6, the substrate bias VBB2 is made to have a desired potential (-1V to 0V) by increasing the number of diodes.

[0080] Referring to Fig. 7B, the substrate bias generating circuit 31 includes a ground terminal GND and an interconnection 31a connected between the ground terminal GND and a substrate bias output terminal VBB2. By the substrate bias generating circuit 31, the substrate bias (0V) at the active state can be generated by the simplest structure.

[0081] Fig. 8 is a schematic diagram showing an example of the bias selecting circuit 32 shown in Fig. 1. Referring to Fig. 8, the bias selecting circuit 32 includes NMOS transistors 321 and 322. The NMOS transistor 321 has its source connected to receive the substrate bias VBB1, its drain connected to the silicon substrate 1 together with the drain of the NMOS transistor 322, and its gate connected to receive the control signal /CNT. The NMOS transistor 322 has its source connected to receive the substrate bias VBB2, and its gate connected to receive the signal CNT.

[0082] In operation, in the standby state, the control signal /CNT is set to the high level, NMOS transistor 321 is turned on, and the substrate bias VBB1 is supplied to the silicon substrate 1. Meanwhile, in the active state, the control signal CNT is set to the high level, the NMOS transistor 322 is turned on, and the substrate bias VBB2 is supplied to the silicon substrate 1. By this simple structure, the substrate bias applied to the silicon substrate 1 can be changed.

[0083] In the bias selecting circuit 32 shown in Fig. 8, the substrate bias is changed in response to the control signal CNT. However, in response to the control signal, input signals Din and /Din may be applied to the gates of the NMOS transistors 321 and 322.

[0084] Fig. 9 is a block diagram of another semiconductor device useful for understanding the invention. Referring to Fig. 9, the semiconductor device differs from the semiconductor device of Fig. 1 in that a CMOS circuit is included in the functional circuit 110, the third and fourth substrate bias circuits 33 and 34 are added, and a bias selecting circuit 32' for selecting the substrate bias VBB2 or VBB4 are provided. Other circuits are the same as those shown in Fig. 1, and therefore they are denoted by the same reference numerals and description thereof is not repeated.

[0085] The third bias generating circuit 33 generates a substrate bias VBB3 in the standby state of the PMOS transistor. The substrate bias VBB3 is set at such a potential as to set the threshold voltage (Vth) of the PMOS transistor at 4.2V. Specifically, it is about 8V. By making this such a deep reverse bias, the leak current in the standby state can be reduced.

[0086] The fourth bias generating circuit 34 generates a substrate bias VBB4 in the active state of the PMOS transistor. The substrate bias VBB4 is determined based on the drivability of supplying current in the active state of the PMOS transistor. More specifically, it is 5V. The drivability of supplying current becomes larger when the threshold voltage Vth is smaller. By determining the threshold voltage, the gate width and the gate length, the current supplying drivability is determined. In this embodiment, the substrate bias VBB4 is set to 5V and the threshold voltage is set to 4.8V, thus increasing the supplying drivability by about 30%.

[0087] Fig. 10 is a cross section of a portion of the semiconductor device shown in Fig. 9. Fig. 11 is a plan view showing a portion of the semiconductor device shown in Fig. 9. The semiconductor device shown in Figs. 10 and 11 constitutes a CMOS circuit including an NMOS transistor and a PMOS transistor combined. Referring to Figs. 10 and 11, the semiconductor device includes a P well 6 doped with P type impurities of 10^{16} to $10^{17}/cm^3$ on a silicon substrate 1, an NMOS transistor 11 formed on the P well 6, an N well 10 doped with N type impurities of 10^{16} to $10^{17}/cm^3$, for example, a PMOS transistor 12 formed on the N well 10, a well terminal 26 to which the substrate bias VBB1 or VBB2 is supplied, and a well terminal 27 to which the substrate bias VBB3 or VBB4 is supplied. The well terminal 26 is connected to the contact hole 26' shown in Fig. 11, and the well terminal 27 is connected to the contact hole 27' shown in Fig. 11.

[0088] Fig. 12 shows changes in the substrate bias (well bias), the threshold voltage and the drivability of supplying current when the semiconductor device shown in Fig. 9 is switched from the standby state to the active state.

[0089] The operation of the semiconductor device shown in Figs. 9 to 11 will be described with reference to Fig. 12. In the standby state, the well bias VBB1 is supplied to the well terminal 26 and the well bias VBB3 is supplied to the well terminal 27, and therefore the threshold voltages Vth are 0.8V and 4.2V, and the drivability of supplying current is 100% as in the prior art. The P well 6 and the source region 2 and the drain region 3 are in the deeply reverse-biased state, and the N well 10 and the source region 8 and the drain region 9 are in the deeply reverse-biased state. Thus the amount of current can be made very small.

[0090] Then, in order to activate the CMOS circuit, the signal CNT is supplied to the bias selecting circuit 32'. In response, the bias selecting circuit 32' selects the substrate bias VBB2 instead of the substrate bias VBB1 to apply this to the well terminal 6, selects the substrate bias VBB4 instead of the substrate bias VBB3 and applies this to the well terminal 27. Consequently, the reverse bias between the P well 6 and each of the source and drain regions 2 and 3 as well as the reverse bias between the N well 10 and each of the source and drain regions 8 and 9 are made shallower. Consequently, the threshold voltages Vth are set to 0.2V and 4.8V, the current supplying drivability is increased to about 130%, and the resistance between the drain region and the source region is made smaller. When a positive voltage is supplied to the gate electrode 5 in this state, the NMOS transistor 11 is turned on quickly, and the PMOS transistor 12 is turned off quickly. Consequently, the speed of operation is increased.

[0091] Fig. 13 is a schematic diagram showing an example of the bias selecting circuit 32' shown in Fig. 9. Referring to Fig. 13, the bias selecting circuit 32' differs from the bias selecting circuit 32 shown in Fig. 8 in that an NMOS transistor 323 responsive to the control signal /CNT for selecting the substrate bias VBB3, and an NMOS transistor 324 responsive to the control signal CNT for selecting the substrate bias VBB4 are added. Other portions are the same as those in Fig. 8.

[0092] Fig. 14 is a cross section showing an embodiment of the semiconductor device in accordance with the present invention. The semiconductor device shown in Fig. 14 has a so called SOI structure. Referring to Fig. 14, the semiconductor device includes a buried insulator layer 14 formed on a silicon substrate 15, an NMOS transistor 11 formed on the buried insulator layer 14, and a PMOS transistor 12 formed on the buried insulator layer 14. Such an SOI-MOSFET is formed by the SIMOX

(Separation by Implanted Oxygen). More specifically, 2 x $10^{18}/cm^2$ of oxygen ions, for example, are implanted to the silicon substrate 15 and thereafter it is heat treated at 1300°C for 6 hours in Ar atmosphere to provide an SOI substrate including three layered structure of silicon/silicon oxide film/silicon. The silicon layer 13 is processed to be islands, and is divided into the NMOS transistor 11 and the PMOS transistor 12. In each of the NMOS transistor 11 and the PMOS transistor 12, a gate electrode 5 is provided with a gate dielectric thin film 4 interposed as in the conventional device formed on the silicon substrate. In the NMOS transistor 11, an N channel region 16 doped with P type impurities of 10^{16} to $10^{17}/cm^3$, for example, is provided in the silicon layer 13 below the gate electrode 5, and the source and drain regions 2 and 3 are provided in the similar manner as the prior art on both sides of the N channel region 16.

[0093] When the gate voltage is applied to the NMOS transistor 11 to activate the transistor, the N channel region 16 is completely depleted, and the impurity concentration of the N channel region 16 is suppressed low, as mentioned above.

[0094] In the PMOS transistor 12, the impurity concentration of the P channel region 17 is made not lower than $10^{17}/cm^3$, which is higher than the NMOS transistor 11, and even when the gate voltage is applied, only a portion of the P channel region 17 is depleted. Except this, the PMOS transistor has similar structure as the NMOS transistor, with the type of impurities opposite to that of NMOS transistor.

[0095] In the SOI-MOSFET, the substrate biases VBB1 and VBB2 are supplied from the rear surface of the silicon substrate 1. The substrate bias VBB1 is fixed at 0V so as to set the threshold voltage Vth at 0.8V, and the potential of the substrate bias VBB2 is 5V so as to set the threshold voltage Vth at 0.2V.

[0096] Fig. 15 shows changes in the threshold voltage and the drivability of supplying current when the substrate bias is changed.

[0097] The operation of the semiconductor device shown in Fig. 14 will be described with reference to Fig. 15.

[0098] The SOI-MOSFET has a MOS structure of silicon substrate 15 / buried oxide layer 14 / silicon layer 13, as viewed from the side of the silicon substrate 15. In other words, MOS structure is formed on both surfaces of the silicon layer 13. The operation when the substrate bias VBB2 (5V) is applied from the silicon substrate 15 changes dependent on whether the channel region is completely depleted or partially depleted when the voltage is applied to the gate. When the channel region is entirely depleted (in this example, NMOS transistor), the capacitors are coupled in series from the buried oxide film 14 to the gate dielectric thin film 4 (buried oxide layer 14 / silicon layer 13 / gate dielectric thin film 4) (capacitance coupled), and the threshold voltages of the MOS transistors 11 and 12 on the top surface side are changed by the substrate bias. The direction of change of the threshold voltages caused by the substrate bias change is the same as that of the MOS transistor formed on the bulk silicon described above. However, since the bias potential is supplied to the semiconductor layer 13 through the thick buried oxide layer 14, the change becomes smaller.

[0099] Let us assume that the channel region is partially depleted, that is, the case of the PMOS transistor. The potential of the channel region which is not depleted is fixed at the potential of the source region 8. Therefore, such a capacitance coupling as occurred when it is fully depleted is not generated. Therefore, the threshold voltage of the MOS on the surface is not influenced by the normal back gate bias.

[0100] In the standby state, the back gate bias VBB1 (substrate bias) is fixed at 0V, and the threshold value is set to suppress current in this state. Thus power consumption can be reduced.

[0101] When the back gate bias is increased from VBB1 to VBB2 (5V) in order to activate the device from the standby state, the threshold value of the NMOS transistor 11 decreases from 0.8V to 0.2V, and hence the drivability of supplying current is increased. By this increase of current, the circuit can operate at higher speed. In the PMOS transistor 12, the channel region is partially depleted, and therefore there is no effect of back gate bias, and the threshold value and the drivability of supplying current are not changed.

[0102] The PMOS transistor 12 is depleted partially so that it is not influence by the back gate bias, since if the NMOS transistor and the PMOS transistor are both fully depleted to be subjected to the back gate bias effect in the SOI-MOSFET, the effects increasing current is reversed in the NMOS transistor and the PMOS transistor. That is, if the back gate bias is applied to increase the current in the NMOS transistor, the drivability of supplying current in the PMOS transistor is reduced.

[0103] In the embodiment shown in Figs. 14 and 15, the NMOS transistor is fully depleted and the PMOS transistor is partially depleted. However, the reverse combination may be available, dependent on the circuit structure. However, if the reverse structure is used, the back gate bias (substrate bias) must be changed in the negative direction, that is, from 5V to 0V, for example.

[0104] Fig. 16 is a cross section showing a further embodiment of the semiconductor device in accordance with the present invention, and Fig. 17 is a plan view of the semiconductor device shown in Fig. 16. In the semiconductor device shown in Figs. 16 and 17, the NMOS transistor and the PMOS transistor are both fully depleted.

[0105] The semiconductor device differs from the semiconductor device shown in Fig. 14 in that an NMOS second gate 18 and a PMOS second gate 19 are provided in the buried oxide film layer. The NMOS second gate 18 is provided below the silicon layer 13 of the NMOS transistor 11, and the PMOS second gate 19 is provided below the PMOS transistor 12.

[0106] Referring to Fig. 17, on the silicon layer 13, a substrate terminal 28 for receiving substrate biases VBB1 and VBB2 and a substrate terminal 29 for receiving mutually complementary substrate biases VBB1 and VBB2 are provided. The potentials of the substrate biases VBB1 and VBB2 are the same as in the embodiment of Fig. 14 (0V, 5V).

[0107] Fig. 18 shows changes in the threshold voltage and the drivability of supplying current when the substrate bias is changed.

[0108] Referring to Fig. 18, the operation of the semiconductor device shown in Figs. 16 and 17 will be described.

[0109] In the standby state, the substrate bias VBB1 (0V) is supplied to the NMOS second gate 18 and the substrate bias VBB2 (5V) is supplied to the PMOS second gate 19 in the standby state. By the application of the substrate biases, the threshold voltage Vth of the NMOS transistor 11 attains 0.8V, and the threshold voltage Vth of the PMOS transistor 12 attains 4.2V, resulting in a deep reverse bias. The operation so far is the same as that of the embodiment shown in Fig. 14.

[0110] When the device is switched from the standby state to the active state, the substrate bias VBB2 is supplied to the NMOS second gate 18, while the substrate bias VBB1 is supplied to the PMOS second gate 19. By the application of the substrate biases, the threshold voltage of the NMOS transistor 11 attains 0.2V, while the threshold voltage of the PMOS transistor 12 attains 4.8V. Thus the drivability of supplying current in the MOS transistors 11 and 12 is increased to about 130%, and consequently, the speed of operation of the CMOS circuit can be increased.

[0111] Fig. 19 shows steps for manufacturing the SOI structure shown in Fig. 16. In Fig. 19(a), a silicon oxide film is formed on the silicon substrate 15, and thereafter a polysilicon layer as the second gates 18 and 19 are formed by sputtering or the like.

[0112] Then, referring to Fig. 19(b), an oxide film is deposited, and thereafter the silicon oxide film is ground by a prescribed thickness (to the dotted line in the figure).

[0113] Then, referring to Fig. 19(c), the silicon layer 40 is deposited.

[0114] Although silicon was used for the semiconductor in the embodiments shown in Figs. 1 to 19, other semiconductor material such as germanium Ge or gallium arsenide GaAs may be used.

[0115] Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being limited only by the terms of the appended claims.

Claims

1. A semiconductor device comprising:

   a semiconductor substrate (15);
   a first conductivity channel type MOS transistor (11) operable selectively in standby and active states, said first conductivity channel type MOS transistor (11) having a first gate electrode (5) and a first channel forming region (16); and
   a back bias driving means (30, 31, 32) for selectively providing a first back bias voltage (VBB1) in the standby state and a second back bias voltage (VBB2) such as to enhance a current supplying drivability of said first conductivity channel type MOS transistor (11) in the active state;

   characterised by

   a second conductivity channel type MOS transistor (12) of opposite channel conductivity type to said first type MOS transistor operable selectively in the standby and active states, said second conductivity channel type MOS transistor (12) having a second gate electrode and a second channel forming region (17); and
   an insulating layer (14) formed on said semiconductor substrate (15); the first and second conductivity channel type MOS transistors (11, 12) being formed on the insulating layer (14).

2. A semiconductor device according to claim 1, wherein said semiconductor substrate (15) has a substrate terminal, and

   said back bias driving means provides said first and second back bias voltages to said substrate terminal.

3. A semiconductor device according to claim 2, wherein said first channel forming region (16) is fully depleted upon application of a threshold voltage thereto, and

   said second channel forming region (17) is partially depleted upon application of a threshold voltage thereto.

4. A semiconductor device according to claim 1, wherein the back bias voltage driving means (30, 31, 32) includes

   first back bias voltage generating means (30) for generating said first back bias voltage (VBB1),
   second back bias voltage generating means (31) for generating said second back bias voltage (VBB2), and
   back bias voltage selecting means (32) coupled

to said first and second back bias generating means (30, 31) for selecting one of said first and second back bias voltages (VBB1, VBB2) provided from said first and second back bias generating means (30, 31) in response to a control signal (CNT) indicative of whether said first and second conductivity channel type MOS transistors (11, 12) are in the standby or active state and providing said selected back bias voltage (VBB1, VBB2) to said first and second conductivity channel type MOS transistors (11, 12).

5. A semiconductor device according to claim 1, wherein said first conductivity channel type MOS transistor is an N channel MOS transistor (11), and
said second conductivity channel type MOS transistor is a P channel MOS transistor (12).

6. A semiconductor device according to claim 5, wherein said N and P channel MOS transistors (11, 12) operate in accordance with power supply and ground voltages (5V, 0V),

said first back bias voltage (VBB1) is equal to said ground voltage (0V), and
said second back bias voltage (VBB2) is equal to said power supply voltage (5V).

7. A semiconductor device according to claim 1, wherein said first conductivity channel type MOS transistor is a P channel MOS transistor (12), and
said second conductivity channel type MOS transistor is an N channel MOS transistor (11).

8. A semiconductor device according to claim 7, wherein said P and N channel MOS transistors (12, 11) operate in accordance with power supply and ground voltages (5V, 0V),

said first back bias voltage (VBB1) is equal to said power supply voltage (5V), and
said second back bias voltage (VBB2) is equal to said ground voltage (0V).

9. A semiconductor device according to claim 5, wherein the first gate electrode (5) is a first front gate electrode (5);

the second gate electrode (5) is a second front gate electrode (5);
and the semiconductor device comprises a first back gate electrode (18) opposite to said first front gate electrode (5) and sandwiching said first channel forming region (16) therebetween;
a second back gate electrode (19) opposite to said second front gate electrode (5) and sandwiching said second channel forming region (17) therebetween;

wherein the back bias driving means (30, 31, 32) is arranged for selectively providing the first back bias voltage (VBB1) and the second back bias voltage (VBB2) to said first back gate electrode (18);

and the device further comprises
a second back bias driving means (32, 33, 34) arranged for selectively providing a third back bias voltage (VBB2) in the standby state and a fourth back bias voltage (VBB1) such as to enhance a current supplying drivability of said P channel MOS transistor (12) in the active state to said second back gate electrode (19).

10. A semiconductor device according to claim 9, wherein said first channel forming region (16) is fully depleted upon application of a threshold voltage thereof, and
said second channel forming region (17) is fully depleted upon application of a threshold voltage thereof.

11. A semiconductor device according to claim 9, wherein said first back bias voltage providing means (30-32) includes

first back bias voltage generating means (30) for generating said first substrate bias voltage (VBB1),
second back bias voltage generating means (31) for generating said second substrate bias voltage (VBB2), and
first back bias voltage selecting means (32) coupled to said first and second back bias voltage generating means (30, 31) and said first back gate electrode (18) for selecting one of said first and second back bias voltages (VBB1, VBB2) provided from said first and second back bias voltage generating means (30, 31) in response to a control signal indicative of whether said N and P channel MOS transistors (11, 12) are in the standby or active state and providing said selected back bias voltage to said first back gate electrode (18), and
said second back bias voltage providing means (32-34) includes
third back bias voltage generating means (33) for generating said third back bias voltage (VBB2),
fourth back bias voltage generating means (34) for generating said fourth back bias voltage (VBB1), and
second back bias voltage selecting means (32) coupled to said third and fourth back bias generating means (33, 34) and said second back gate electrode (19) for selecting one of said third and fourth back bias voltages (VBB2,

VBB1) provided from said third and fourth back bias voltage generating means (33, 34) in response to said control signal (CNT) and providing said selected back bias voltage to said second back gate electrode (19).

12. A semiconductor device according to claim 9, wherein said N and P channel MOS transistors (11, 12) operate in accordance with power supply and ground voltages (5V, 0V), said first back bias voltage (VBB1) is equal to said ground voltage (0V),

said second back bias voltage (VBB2) is equal to said power supply voltage (5V),
said third back bias voltage (VBB2) is equal to said power supply voltage (5V), and
said fourth back bias voltage (VBB1) is equal to said ground voltage (0V).

13. A semiconductor device according to claim 9, wherein said first and second back gate electrodes (18, 19) are buried in said insulating layer (14).

14. A semiconductor device according to any one of claims 1 to 13, wherein said standby state is off state, and said active state is on state.

Patentansprüche

1. Halbleitervorrichtung mit

einem Halbleitersubstrat (15);
einem ersten MOS-Transistor (11) mit einem Kanal eines Leitfähigkeitstyps, der in einem Bereitschaftszustand und in einem aktiven Zustand selektiv betreibbar ist, wobei der erste MOS-Transistor (11) mit einem Kanal eines Leitfähigkeitstyps eine erste Gateelektrode (5) und einen ersten Kanalbildungsbereich (16) aufweist; und
einem Rückwärtsvorspannungs-Antriebsmittel (30, 31, 32) zum selektiven Vorsehen einer ersten Rückwärtsvorspannungsspannung (VBB1) in dem Bereitschaftszustand und einer zweiten Rückwärtsvorspannungsspannung (VBB2) derart, daß eine Stromlieferungs-Treiberfähigkeit des ersten MOS-Transistors (11) mit einem Kanal eines Leitfähigkeitstyps in dem aktiven Zustand erhöht ist;

gekennzeichnet durch

einen zweiten MOS-Transistor (12) mit einem Kanal eines Leitfähigkeitstyps eines dem ersten Typ-MOS-Transistor entgegengesetzten Kanalleitfähigkeitstyps, der selektiv in dem Bereitschaftszustand und in dem aktiven Zustand betreibbar ist, wobei der zweite MOS-Transistor (12) mit einem Kanal eines Leitfähigkeitstyps eine zweite Gateelektrode und einen zweiten Kanalbildungsbereich (17) aufweisen; und
einer Isolierschicht (14), die auf dem Halbleitersubstrat (15) gebildet ist; wobei der erste MOS-Transistor (11) mit einem Kanal eines Leitfähigkeitstyps und der zweite MOS-Transistor (12) mit einem Kanal eines Leitfähigkeitstyps auf der Isolierschicht (14) gebildet ist.

2. Halbleitervorrichtung nach Anspruch 1, in der das Halbleitersubstrat (15) einen Substratanschluß aufweist, und das Rückwärtsvorspannungsantriebsmittel die erste und die zweite Rückwärtsvorspannungsspannung an den Substratanschluß liefert.

3. Halbleitervorrichtung nach Anspruch 2, in der der erste Kanalbildungsbereich (16) beim Anlegen einer Schwellenspannung daran vollständig verarmt wird, und
der zweite Kanalbildungsbereich (17) teilweise beim Anlegen einer Schwellenspannung daran verarmt wird.

4. Halbleitervorrichtung nach Anspruch 1, in der das Rückwärtsvorspannungsspannungsantriebsmittel (30, 31, 32) ein erstes Rückwärtsvorspannungsspannung-Erzeugungsmittel (30) zum Erzeugen der ersten Rückwärtsvorspannungsspannung (VBB1), ein zweites Rückwärtsvorspannungsspannung-Erzeugungsmittel (31) zum Erzeugen der zweiten Rückwärtsvorspannungsspannung (VBB2), und ein Rückwärtsvorspannungsspannungsauswahlmittel (32), das mit dem ersten und dem zweiten Rückwärtsvorspannungs-Erzeugungsmittel (30, 31) gekoppelt ist, zum Auswählen einer der ersten und zweiten Rückwärtsvorspannungsspannungen (VBB1, VBB2), die von dem ersten und zweiten Rückwärtsvorspannungs-Erzeugungsmittel (30, 31) als Reaktion auf ein Steuersignal (CNT) geliefert wird, welches bezeichnend dafür ist, ob der erste MOS-Transistor (11) mit einem Kanal eines Leitfähigkeitskanaltyps und der zweite MOS-Transistor (12) mit einem Kanal eines Leitfähigkeitskanaltyps sich in dem Bereitschaftszustand oder in dem aktiven Zustand befinden, und Liefern der ausgewählten Rückwärtsvorspannungsspannung (VBB1, VBB2) an den ersten MOS-Transistor (11) mit einem Kanal eines Leitfähigkeitskanaltyps und den zweiten MOS-Transistor (12) mit einem Kanal eines Leitfähigkeitskanaltyps aufweist.

5. Halbleitervorrichtung nach Anspruch 1, in der der erste MOS-Transistor mit einem Kanal eines Leitfähigkeitstyps ein N-Kanal-MOS-Transistor (11) ist, und
der zweite MOS-Transistor mit einem Kanal eines

Leitfähigkeitstyps ein P-Kanal-MOS-Transistor (12) ist.

6. Halbleitervorrichtung nach Anspruch 5, in der die N- und P-Kanal-MOS-Transistoren (11, 12) gemäß einer Stromversorgungsspannung und einer Massenspannung (5V, 0V) arbeitet,

die erste Rückwärtsvorspannungsspannung (VBB1) gleich der Massenspannung (0V) ist, und
die zweite Rückwärtsvorspannungsspannung (VBB2) gleich der Stromversorgungsspannung (5V) ist.

7. Halbleitervorrichtung nach Anspruch 1, in der der erste MOS-Transistor mit einem Kanal eines Leitfähigkeitstyps ein P-Kanal-MOS-Transistor (12) ist, und
der zweite MOS-Transistor mit einem Kanal eines Leitfähigkeitstyps ein N-Kanal-MOS-Transistor (11) ist.

8. Halbleitervorrichtung nach Anspruch 7, in der die P- und N-Kanal-MOS-Transistoren (12, 11) gemäß einer Stromversorgungsspannung und einer Massenspannung (5V, 0V) arbeiten,

die erste Rückwärtsvorspannungsspannung (VBB1) gleich der Stromversorgungsspannung (5V) ist, und
die zweite Rückwärtsvorspannungsspannung (VBB2) der Massenspannung (0V) ist.

9. Halbleitervorrichtung nach Anspruch 5, in der die erste Gateelektrode (5) sich in einer ersten Frontgate-Elektrode (5) befindet;

die zweite Gateelektrode (5) sich in einer zweiten Frontgate-Elektrode (5) befindet;
und die Halbleitervorrichtung eine erste Backgate-Elektrode (18) aufweist, welche der ersten Frontgate-Elektrode (5) entgegengesetzt ist und den ersten Kanalbildungsbereich (16) dazwischen anordnet;
einer zweiten Backgate-Elektrode (19), welche der zweiten Frontgate-Elektrode 5 entgegengesetzt ist und den zweiten Kanalbildungsbereich (17) dazwischen anordnet;
wobei das Rückwärtsvorspannungsantriebsmittel (30, 31, 32) zum selektiven Liefern der ersten Rückwärtsvorspannungsspannung (VBB1) und der zweiten Rückwärtsvorspannungsspannung (VBB2) an die erste Backgate-Elektrode (18) angeordnet ist;
und die Vorrichtung ferner
ein zweites Rückwärtsvorspannungsantriebsmittel (32, 33, 34) aufweist, das angeordnet ist zum selektiven Liefern einer dritten Rückwärtsvorspannungsspannung (VBB2) in dem Bereitschaftszustand und einer vierten Rückwärtsvorspannungsspannung (VBB1) derart, daß eine Stromlieferungs-Treiberfähigkeit des P-Kanal-MOS-Transistors (12) in dem aktiven Zustand an die zweite Backgate-Elektrode (19) erhöht ist.

10. Halbleitervorrichtung nach Anspruch 9, in der der erste Kanalbildungsbereich (16) vollständig beim Anlegen einer Schwellenspannung davon verarmt wird, und
der zweite Kanalbildungsbereich (17) vollständig beim Anlegen einer Schwellenspannung davon verarmt wird.

11. Halbleitervorrichtung nach Anspruch 9, in der das erste Rückwärtsvorspannungsspannungs-Liefermittel (30 bis 32)

ein erstes Rückwärtsvorspannungsspannungs-Erzeugungsmittel (30) zum Erzeugen der ersten Substratvorspannungsspannung (VBB1), ein zweites Rückwärtsvorspannungsspannungs-Erzeugungsmittel (31) zum Erzeugen der zweiten Substratvorspannungsspannung (VBB2), und
ein erstes Rückwärtsvorspannungsspannungs-Auswahlmittel (32), welches mit dem ersten und zweiten Rückwärtsvorspannungsspannungs-Erzeugungsmittel (30, 31) und der ersten Backgate-Elektrode (18) gekoppelt ist, zum Auswählen einer der ersten und zweiten Rückwärtsvorspannungsspannungen (VBB1, VBB2), welche von dem ersten und zweiten Rückwärtsvorspannungsspannungs-Erzeugungsmittel (30, 31) als Reaktion auf ein Steuersignal geliefert wird, daß dafür bezeichnend ist, ob der N- und der P-Kanal-MOS-Transistor (11, 12) sich in dem Bereitschaftszustand oder in dem aktiven Zustand befinden, und Liefern der ausgewählten Rückwärtsvorspannung an die erste Backgate-Elektrode (18) aufweist und das zweite Rückwärtsvorspannungsspannung-Liefermittel (32 - 34) ein drittes Rückwärtsvorspannungsspannung-Erzeugungsmittel (33) zum Erzeugen der dritten Rückwärtsvorspannungsspannung (VBB2), ein viertes Rückwärtsvorspannungsspannungs-Erzeugungsmittel (34) zum Erzeugen der vierten Rückwärtsvorspannungsspannung (VBB1), und
ein zweites Rückwärtsvorspannungsspannungs-Auswahlmittel (32), welches mit dem dritten und vierten Rückwärtsvorspannungsspannungs-Erzeugungsmittel (33, 34) und der zweiten Backgate-Elektrode (19) gekoppelt ist,

zum Auswählen einer der dritten und vierten Rückwärtsvorspannungsspannungen (VBB2, VBB1), die von den dritten und vierten Rückwärtsvorspannungsspannungs-Erzeugungsmittel (33, 34) als Reaktion auf das Steuersignal (CNT) geliefert werden, und zum Liefern der ausgewählten Rückwärtsvorspannungsspannung an die zweite Backgate-Elektrode (19) aufweist.

12. Halbleitervorrichtung nach Anspruch 9, in der die N- und P-Kanal-MOS-Transistoren (11, 12) gemäß der Stromversorgungsspannung und der Massenspannung (5V, 0V) arbeiten, die erste Rückwärtsvorspannungsspannung (VBB1) der Massenspannung (0V) gleich ist,

die zweite Rückwärtsvorspannungsspannung (VBB2) der Stromversorgungsspannung (5V) gleich ist,
die dritte Rückwärtsvorspannungsspannung (VBB2) der Stromversorgungsspannung (5V) gleich ist, und
die vierte Rückwärtsvorspannungsspannung (VBB1) der Massenspannung (0V) gleich ist.

13. Halbleitervorrichtung nach Anspruch 9, in der die erste und zweite Backgate-Elektrode (18, 19) in der Isolierschicht (14) vergraben sind.

14. Halbleitervorrichtung nach einem der Ansprüche 1 bis 13, bei der der Bereitschaftszustand ein Aus-Zustand, und der aktive Zustand ein Ein-Zustand ist.

Revendications

1. Un dispositif à semiconducteur comprenant :

un substrat semiconducteur (15);
un transistor MOS (11) d'un premier type de conductivité de canal qu'on peut faire fonctionner sélectivement dans des états d'attente et actif, le transistor MOS (11) du premier type de conductivité de canal ayant une première électrode de grille (5) et une première région de formation de canal (16); et
un moyen d'attaque de polarisation arrière (30, 31, 32) pour fournir sélectivement une première tension de polarisation arrière (VBB1) dans l'état d'attente et une seconde tension de polarisation arrière (VBB2), de façon à renforcer une possibilité de fourniture de courant du transistor MOS (11) du premier type de conductivité de canal dans l'état actif;

caractérisé par

un transistor MOS (12) d'un second type de conductivité de canal, opposé au type de conductivité de canal du transistor MOS du premier type, qu'on peut faire fonctionner sélectivement dans les états d'attente et actif, ce transistor MOS (12) du second type de conductivité de canal ayant une seconde électrode de grille et une seconde région de formation de canal (17); et
une couche isolante (14) formée sur le substrat semiconducteur (15); les transistors MOS (11, 12) des premier et second types de conductivité de canal étant formés sur la couche isolante (14).

2. Un dispositif à semiconducteur selon la revendication 1, dans lequel le substrat semiconducteur (15) a une borne de substrat, et
les moyens d'attaque de polarisation arrière appliquent les première et seconde tensions de polarisation arrière à la borne de substrat.

3. Dispositif à semiconducteur selon la revendication 2, dans lequel la première région de formation de canal (16) est placée dans un état de déplétion complète lorsqu'une tension de seuil lui est appliquée, et
la seconde région de formation de canal (17) est placée dans un état de déplétion partielle lorsqu'une tension de seuil lui est appliquée.

4. Un dispositif à semiconducteur selon la revendication 1, dans lequel les moyens d'attaque de tension de polarisation arrière (30, 31, 32) comprennent :

un premier moyen de génération de tension de polarisation arrière (30) pour générer la première tension de polarisation arrière (VBB1),
un second moyen de génération de tension de polarisation arrière (31) pour générer la seconde tension de polarisation arrière (VBB2), et
un moyen de sélection de tension de polarisation arrière (32) connecté aux premier et second moyens de génération de polarisation arrière (30, 31) pour sélectionner l'une des première et seconde tensions de polarisation arrière (VBB1, VBB2) qui sont fournies par les premier et second moyens de génération de polarisation arrière (30, 31), en réponse à un signal de commande (CNT) indiquant si les transistors MOS (11, 12) des premier et second types de conductivité de canal sont dans l'état d'attente ou dans l'état actif, et pour appliquer la tension de polarisation arrière (VBB1, VBB2) sélectionnée aux transistors MOS (11, 12) des premier et second types de conductivité de canal.

5. Un dispositif à semiconducteur selon la revendication 1, dans lequel le transistor MOS du premier type de conductivité de canal est un transistor MOS à canal N (11), et

le transistor MOS du second type de conductivité de canal est un transistor MOS à canal P (12).

6. Un dispositif à semiconducteur selon la revendication 5, dans lequel les transistors MOS à canal N et P (11, 12) fonctionnent conformément à des tensions d'alimentation et de masse (5V, 0V),

la première tension de polarisation arrière (VBB1) est égale à la tension de masse (0V), et la seconde tension de polarisation arrière (VBB2) est égale à la tension d'alimentation (5V).

7. Un dispositif à semiconducteur selon la revendication 1, dans lequel le transistor MOS du premier type de conductivité de canal est un transistor MOS à canal P (12), et

le transistor MOS du second type de conductivité de canal est un transistor MOS à canal N (11).

8. Un dispositif à semiconducteur selon la revendication 7, dans lequel les transistors MOS à canal P et N (12, 11) fonctionnent conformément à des tensions d'alimentation et de masse (5V, 0V),

la première tension de polarisation arrière (VBB1) est égale à la tension d'alimentation (5V), et
la seconde tension de polarisation arrière (VBB2) est égale à la tension de masse (0V).

9. Un dispositif à semiconducteur selon la revendication 5, dans lequel la première électrode de grille (5) est une première électrode de grille avant (5);

la seconde électrode de grille (5) est une seconde électrode de grille avant (5);
et le dispositif à semiconducteur comprend une première électrode de grille arrière (18) disposée face à la première électrode de grille avant (5) avec la première région de formation de canal (16) interposée entre elles;
une seconde électrode de grille arrière (19) disposée face à la seconde électrode de grille avant (5) avec la seconde région de formation de canal (17) interposée entre elles;
dans lequel les moyens d'attaque de polarisation arrière (30, 31, 32) sont conçus pour appliquer sélectivement la première tension de polarisation arrière (VBB1) et la seconde tension de polarisation arrière (VBB2) à la première électrode de grille arrière (18);
et le dispositif comprend en outre des seconds moyens d'attaque de polarisation arrière (32, 33, 34) conçus pour appliquer sélectivement à la seconde électrode de grille arrière (19) une troisième tension de polarisation arrière (VBB2) dans l'état d'attente et une quatrième tension de polarisation arrière (VBB1), de façon à renforcer une possibilité de fourniture de courant du transistor MOS à canal P (12) dans l'état actif.

10. Un dispositif à semiconducteur selon la revendication 9, dans lequel la première région de formation de canal (16) est placée dans un état de déplétion complète sous l'effet de l'application d'une tension de seuil de cette région, et

la seconde région de formation de canal (17) est placée dans un état de déplétion complète sous l'effet de l'application d'une tension de seuil de cette région.

11. Un dispositif à semiconducteur selon la revendication 9, dans lequel les premiers moyens d'application de tension de polarisation arrière (30-32) comprennent :

un premier moyen de génération de tension de polarisation arrière (30) pour générer la première tension de polarisation de substrat (VBB1),
un second moyen de génération de tension de polarisation arrière (31) pour générer la seconde tension de polarisation de substrat (VBB2), et
un premier moyen de sélection de tension de polarisation arrière (32) couplé aux premier et second moyens de génération de tension de polarisation arrière (30, 31) et à la première électrode de grille arrière (18) pour sélectionner l'une des première et seconde tensions de polarisation arrière (VBB1, VBB2) qui sont fournies par les premier et second moyens de génération de tension de polarisation arrière (30, 31), en réponse à un signal de commande indiquant si les transistors MOS à canal N et P (11, 12) sont dans l'état d'attente ou l'état actif, et pour appliquer la tension de polarisation arrière sélectionnée à la première électrode de grille arrière (18), et
les seconds moyens d'application de tension de polarisation arrière (32-34) comprennent
un troisième moyen de génération de tension de polarisation arrière (33) pour générer la troisième tension de polarisation arrière (VBB2),
un quatrième moyen de génération de tension de polarisation arrière (34) pour générer la quatrième tension de polarisation arriève (VBB1), et
un second moyen de sélection de tension de polarisation arrière (32) connecté aux troisième

et quatrième moyens de génération de polarisation arrière (33, 34) et à la seconde électrode de grille arrière (19) pour sélectionner des troisième et quatrième tensions de polarisation arrière (VBB2, VBB1) qui sont fournies par les troisième et quatrième moyens de génération de tension de polarisation arrière (33, 34), en réponse au signal de commande (CNT), et pour appliquer la tension de polarisation arrière sélectionnée à la seconde électrode de grille arrière (19).

12. Un dispositif à semiconducteur selon la revendication 9, dans lequel les transistors MOS à canal N et P (11, 12) fonctionnent conformément à des tensions d'alimentation et de masse (5V, 0V), la première tension de polarisation arrière (VBB1) est égale à la tension de masse (0V),

la seconde tension de polarisation arrière (VBB2) est égale à la tension d'alimentation (5V),
la troisième tension de polarisation arrière (VBB2) est égale à la tension d'alimentation (5V), et
la quatrième tension de polarisation arrière (VBB1) est égale à la tension de masse (0V).

13. Un dispositif à semiconducteur selon la revendication 9, dans lequel les première et seconde électrodes de grille arrière (18, 19) sont enterrées dans la couche isolante (14).

14. Un dispositif à semiconducteur selon l'une quelconque des revendications 1 à 13, dans lequel l'état d'attente est l'état bloqué, et l'état actif est l'état conducteur.

FIG. 1

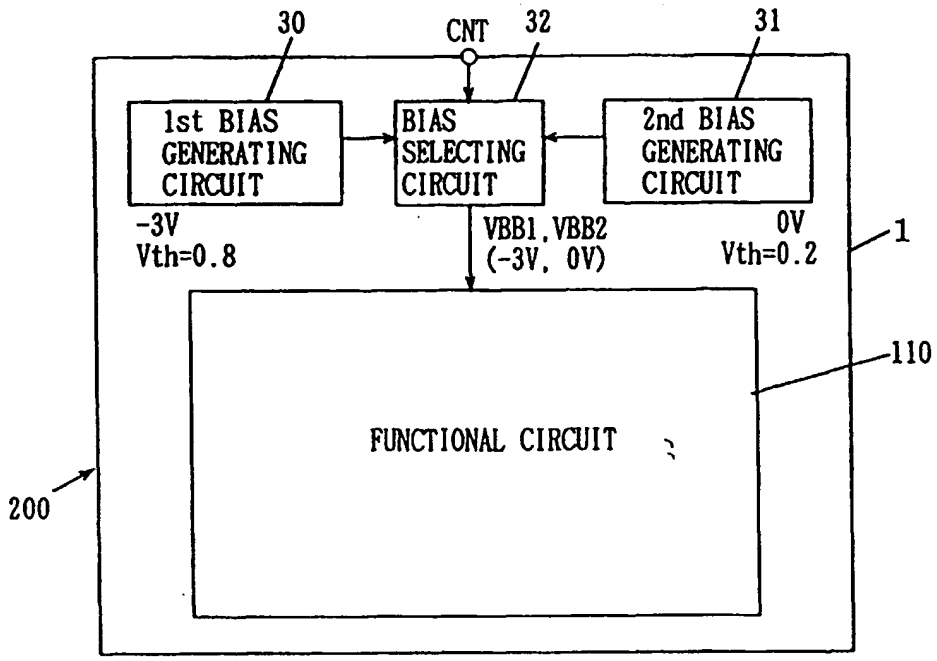
30
CNT
32
31
1st BIAS GENERATING CIRCUIT
BIAS SELECTING CIRCUIT
2nd BIAS GENERATING CIRCUIT
-3V
Vth=0.8
VBB1, VBB2
(-3V, 0V)
0V
Vth=0.2
1
110
FUNCTIONAL CIRCUIT
200

FIG. 2

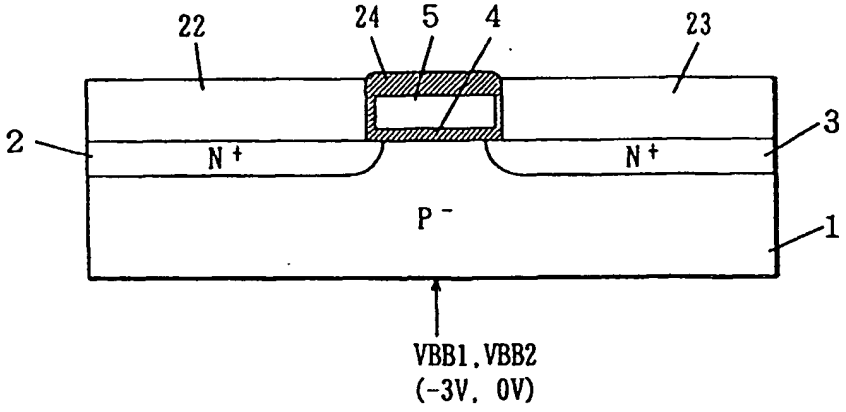
22
24
5
4
23
2
3
N+
N+
P-
1
VBB1, VBB2
(-3V, 0V)

FIG. 3

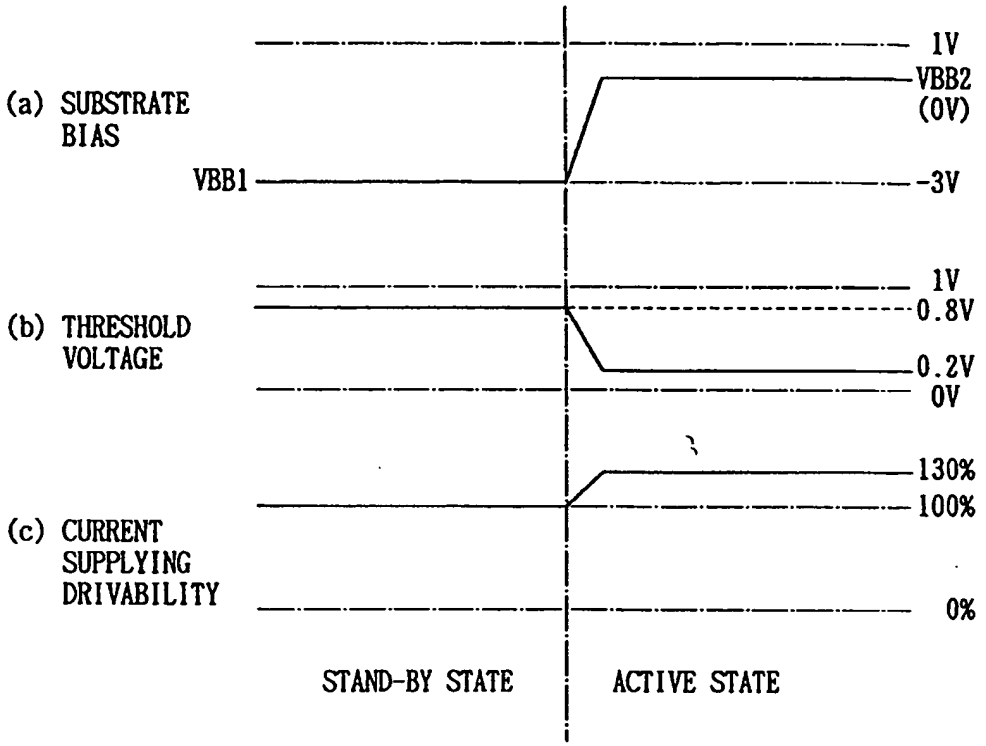
(a) SUBSTRATE BIAS
VBB1
1V
VBB2 (0V)
-3V
(b) THRESHOLD VOLTAGE
1V
0.8V
0.2V
0V
(c) CURRENT SUPPLYING DRIVABILITY
130%
100%
0%
STAND-BY STATE
ACTIVE STATE

FIG. 4A

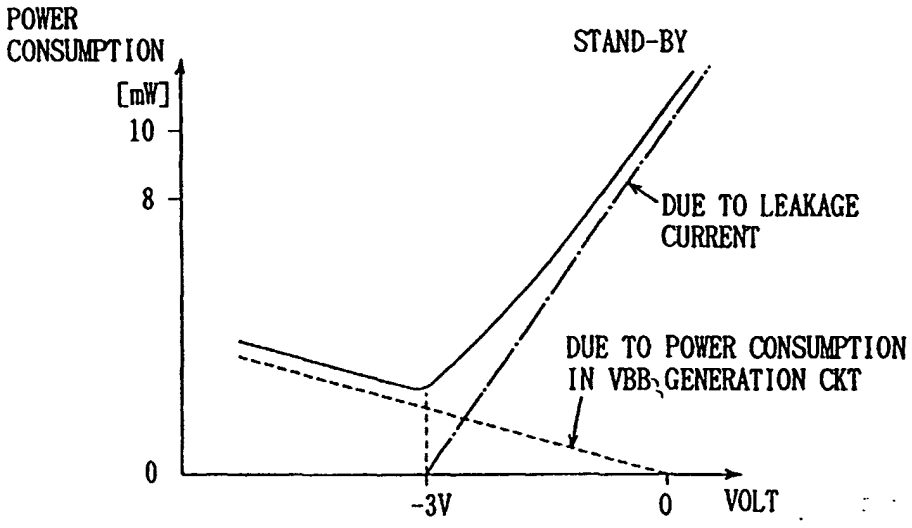
POWER
CONSUMPTION
[mW]
10
8
0
STAND-BY
DUE TO LEAKAGE
CURRENT
DUE TO POWER CONSUMPTION
IN VBB GENERATION CKT
-3V
0
VOLT

FIG. 4B

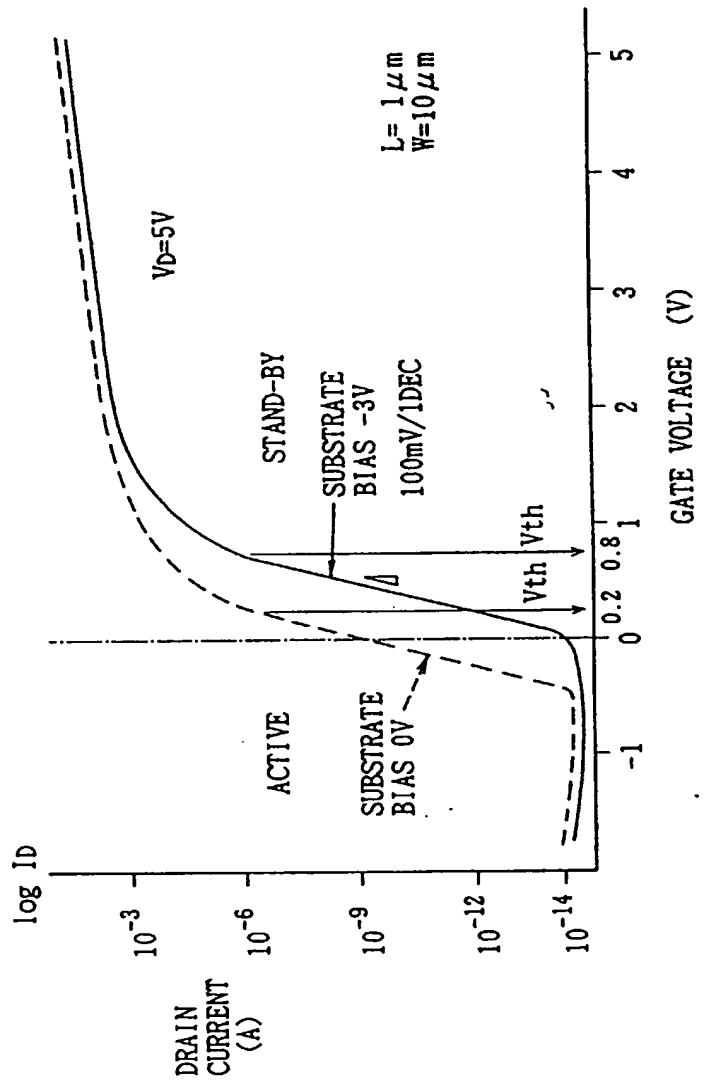
log ID
DRAIN CURRENT (A)
10^{-3}
10^{-6}
10^{-9}
10^{-12}
10^{-14}
ACTIVE
SUBSTRATE BIAS 0V
STAND-BY
SUBSTRATE BIAS -3V
100mV/1DEC
VD=5V
L= 1μm
W=10μm
Vth
Vth
-1
0
0.2
0.8
1
2
3
4
5
GATE VOLTAGE (V)

FIG. 5A

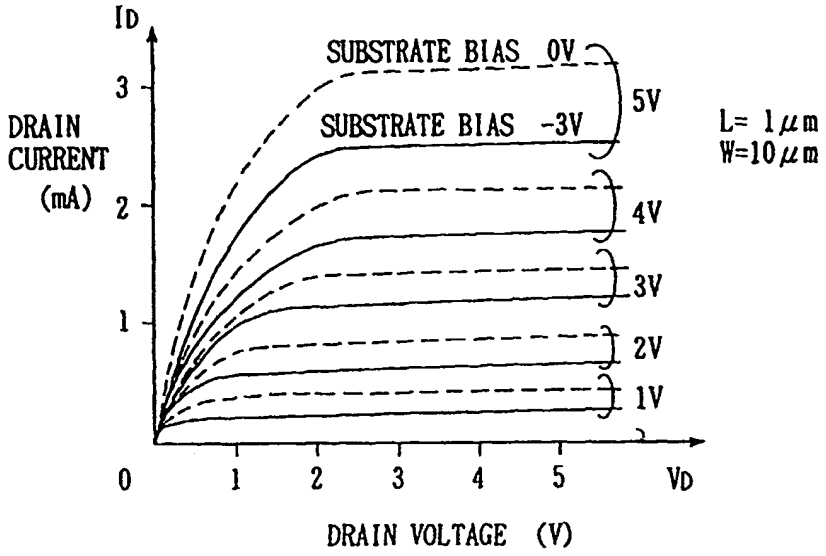
ID
DRAIN CURRENT (mA)
SUBSTRATE BIAS 0V
SUBSTRATE BIAS -3V
5V
4V
3V
2V
1V
L= 1μm
W=10μm
0
1
2
3
4
5
VD
DRAIN VOLTAGE (V)

FIG. 5B

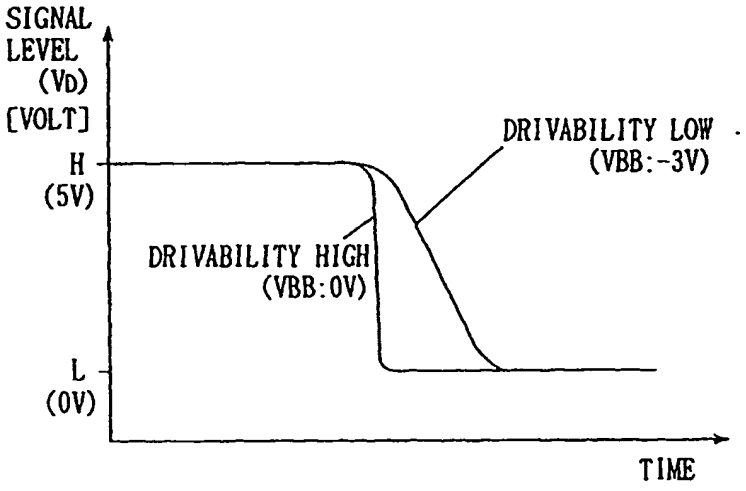
SIGNAL LEVEL (VD) [VOLT]
H (5V)
L (0V)
DRIVABILITY LOW (VBB:-3V)
DRIVABILITY HIGH (VBB:0V)
TIME

FIG. 6

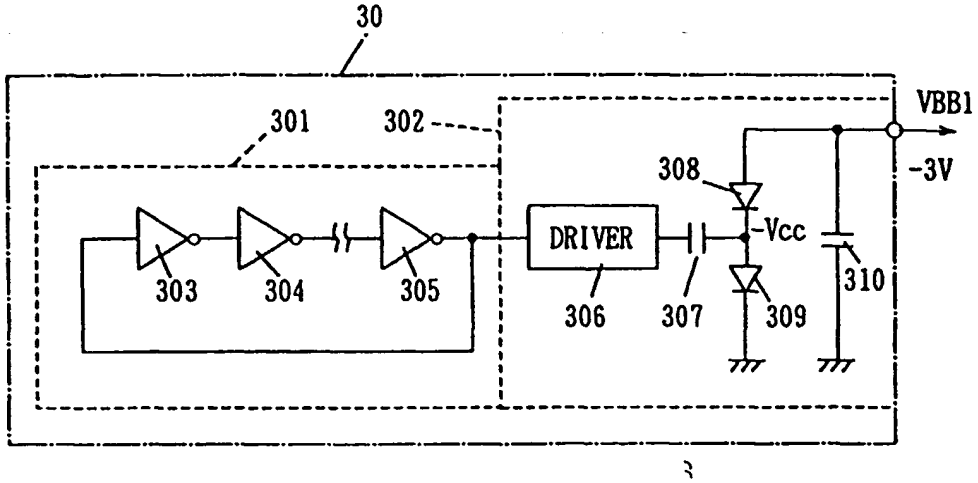

FIG. 7A

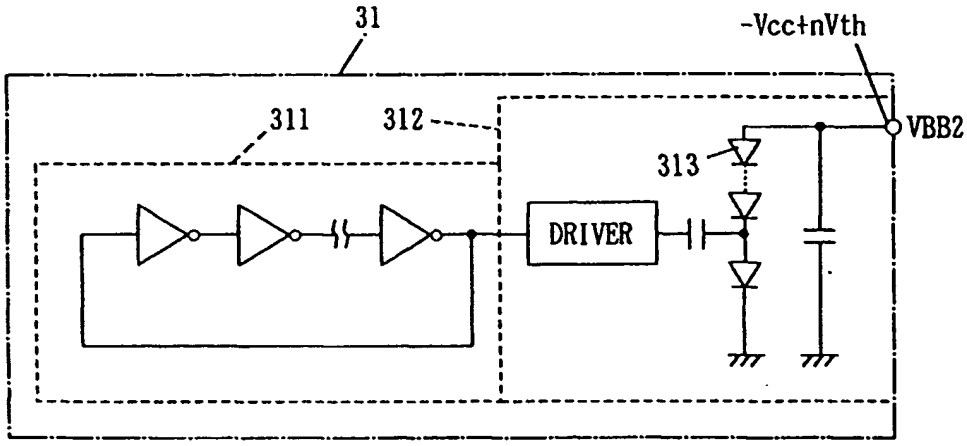

FIG. 7B

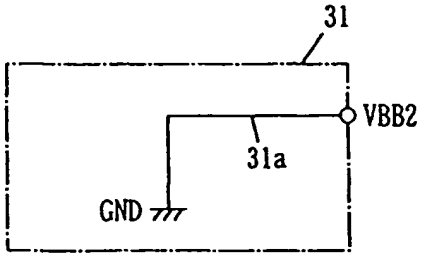

FIG. 8

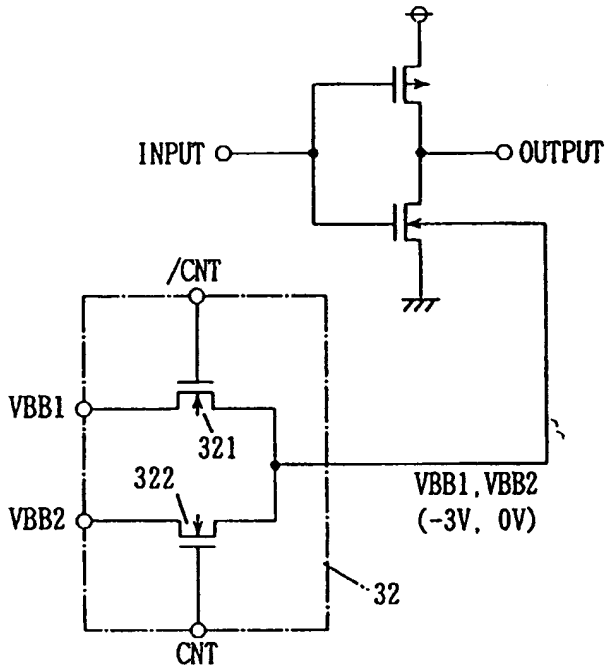

FIG. 9

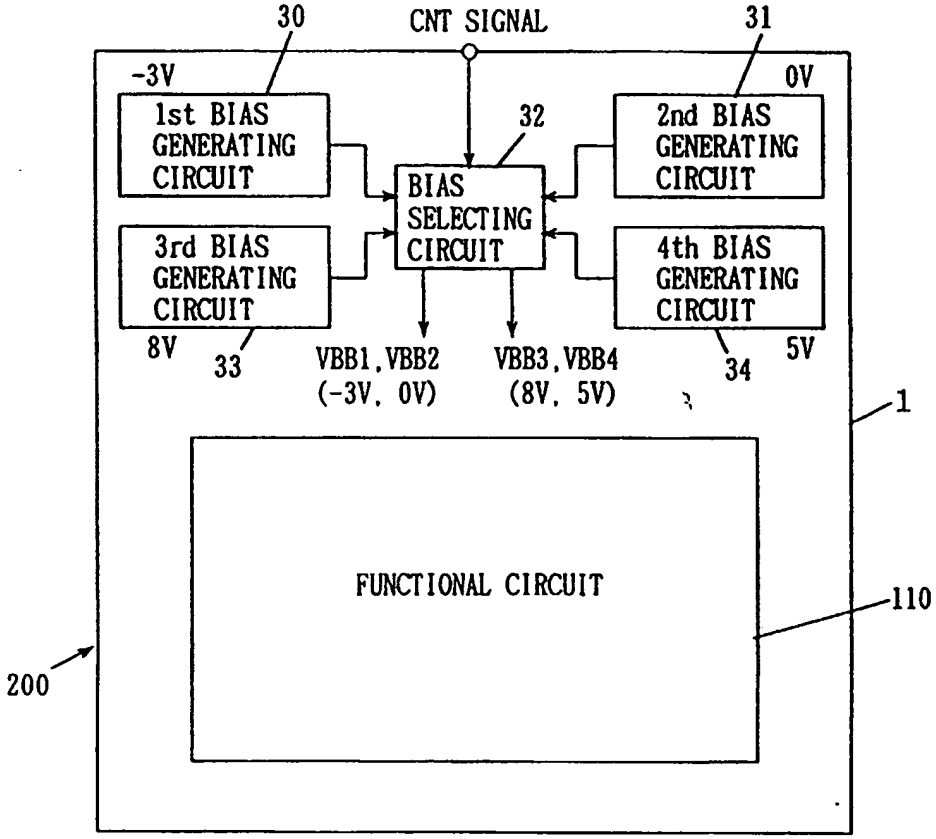
30
CNT SIGNAL
31
-3V
0V
1st BIAS GENERATING CIRCUIT
32
2nd BIAS GENERATING CIRCUIT
BIAS SELECTING CIRCUIT
3rd BIAS GENERATING CIRCUIT
4th BIAS GENERATING CIRCUIT
8V
33
VBB1, VBB2 (-3V, 0V)
VBB3, VBB4 (8V, 5V)
34
5V
1
FUNCTIONAL CIRCUIT
110
200

FIG. 10

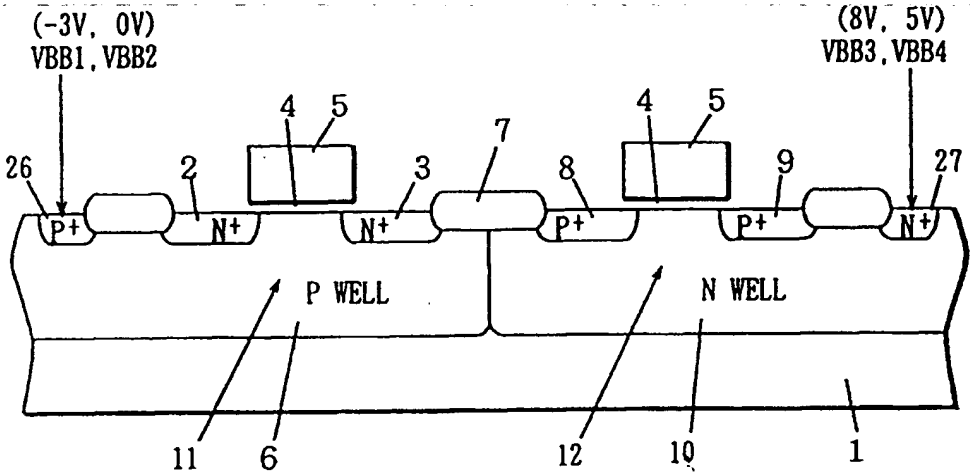
(-3V, 0V)
VBB1, VBB2
(8V, 5V)
VBB3, VBB4
26
2
4
5
3
7
8
4
5
9
27
P+
N+
N+
P+
P+
N+
P WELL
N WELL
11
6
12
10
1

FIG. 11

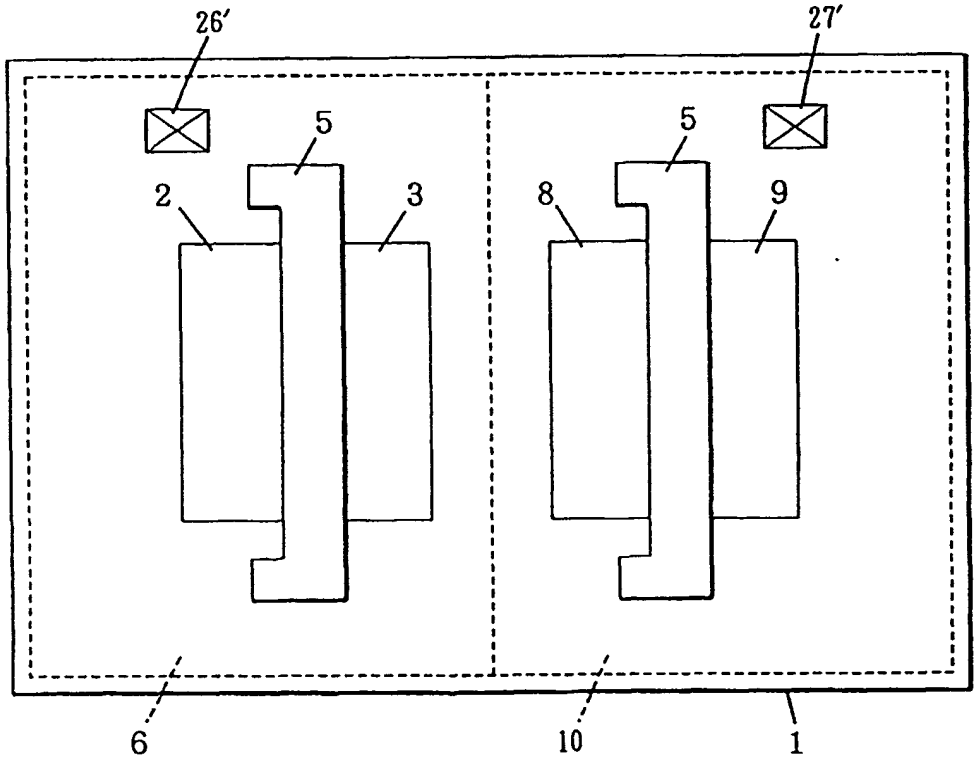
26'
27'
5
5
2
3
8
9
6
10
1

FIG. 12

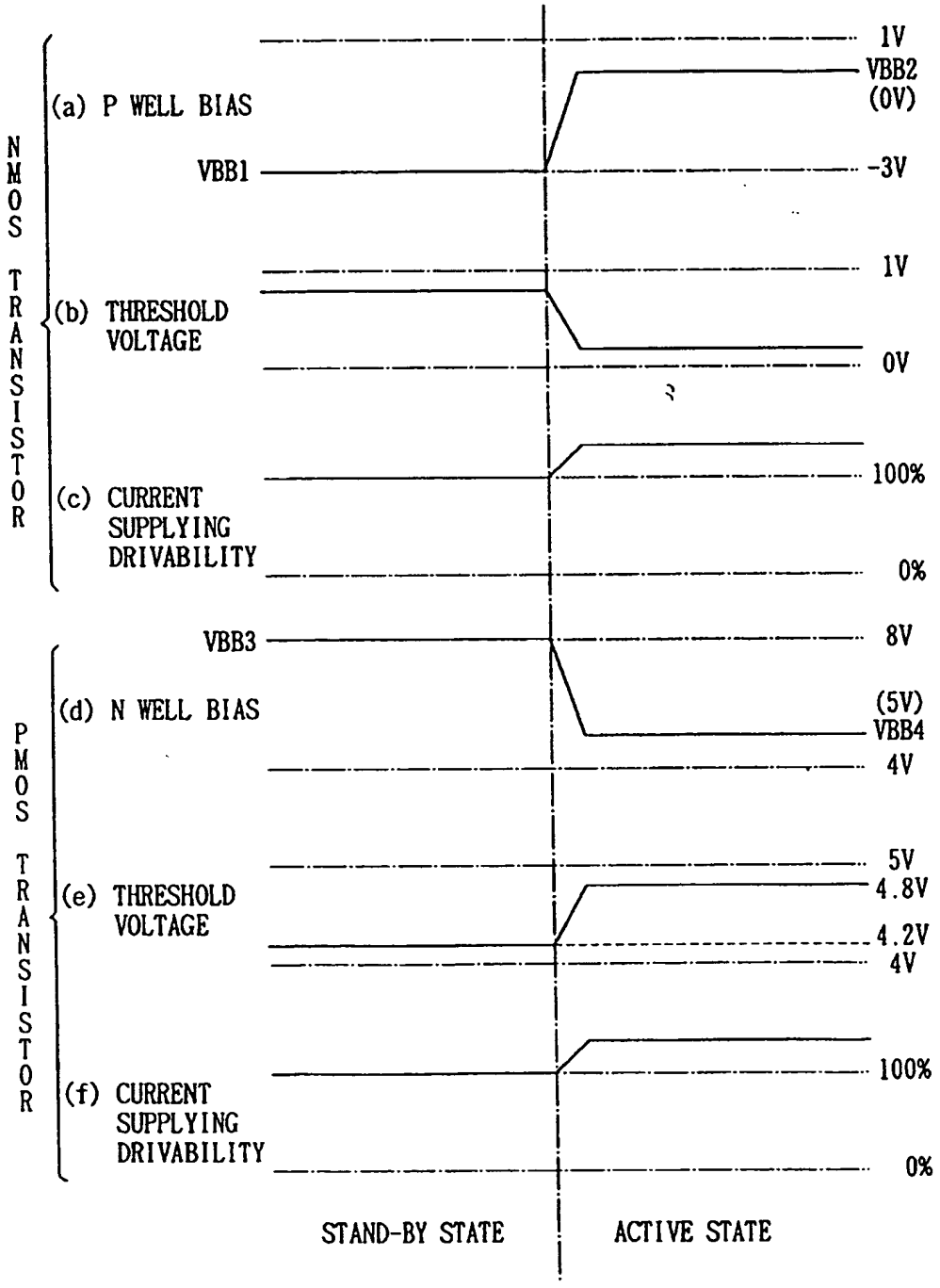
NMOS TRANSISTOR
(a) P WELL BIAS
VBB1
1V
VBB2
(0V)
-3V
(b) THRESHOLD VOLTAGE
1V
0V
(c) CURRENT SUPPLYING DRIVABILITY
100%
0%
PMOS TRANSISTOR
VBB3
8V
(d) N WELL BIAS
(5V)
VBB4
4V
(e) THRESHOLD VOLTAGE
5V
4.8V
4.2V
4V
(f) CURRENT SUPPLYING DRIVABILITY
100%
0%
STAND-BY STATE
ACTIVE STATE

FIG. 13

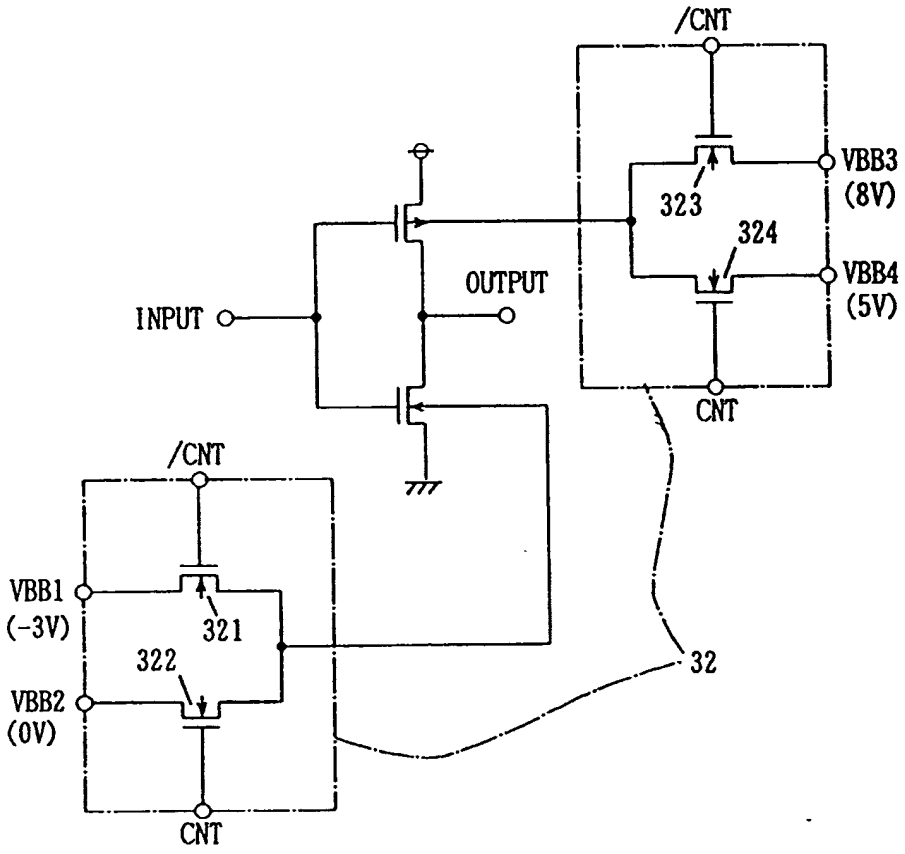
/CNT
VBB3
(8V)
323
324
VBB4
(5V)
OUTPUT
INPUT
CNT
/CNT
VBB1
(-3V)
321
322
VBB2
(0V)
32
CNT

FIG. 14

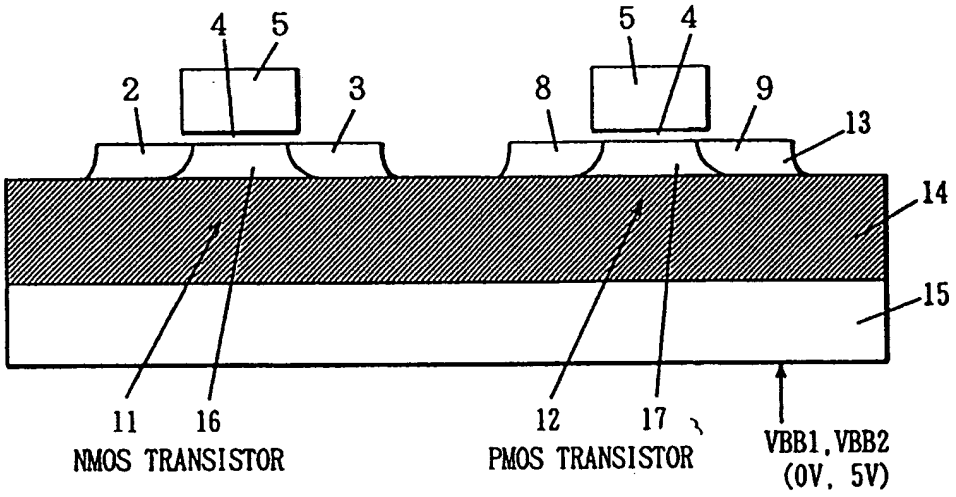
4
5
5
4
2
3
8
9
13
14
15
11
16
12
17
NMOS TRANSISTOR
PMOS TRANSISTOR
VBB1, VBB2
(0V, 5V)

FIG. 15

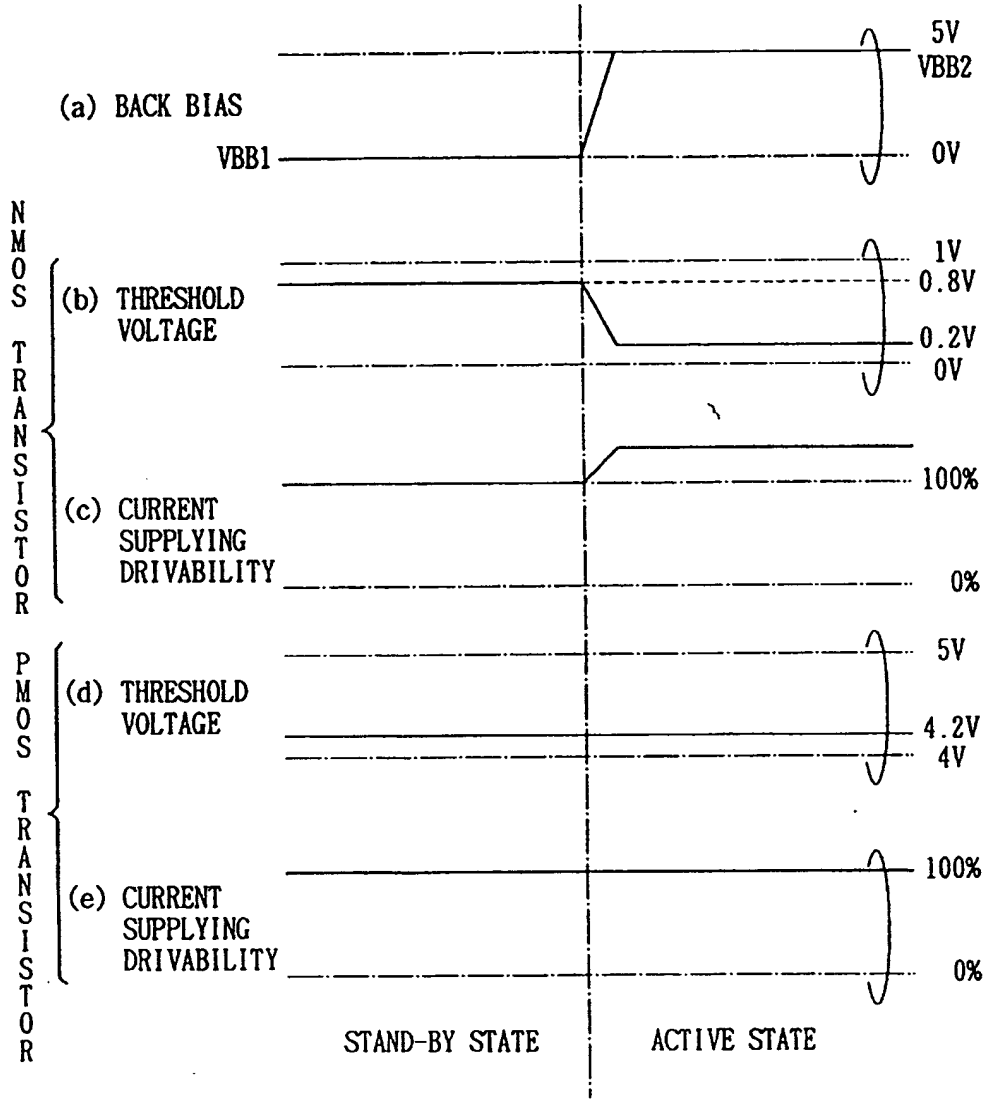
(a) BACK BIAS
VBB1
5V
VBB2
0V
NMOS TRANSISTOR
(b) THRESHOLD VOLTAGE
1V
0.8V
0.2V
0V
(c) CURRENT SUPPLYING DRIVABILITY
100%
0%
PMOS TRANSISTOR
(d) THRESHOLD VOLTAGE
5V
4.2V
4V
(e) CURRENT SUPPLYING DRIVABILITY
100%
0%
STAND-BY STATE
ACTIVE STATE

FIG. 16

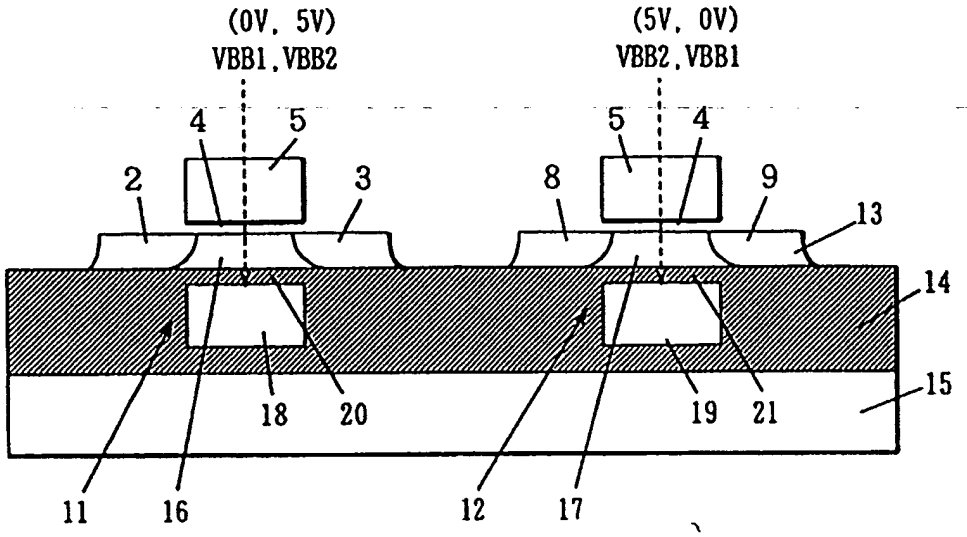
(0V, 5V)
VBB1, VBB2
(5V, 0V)
VBB2, VBB1
4
5
5
4
2
3
8
9
13
14
15
18
20
19
21
11
16
12
17

FIG. 17

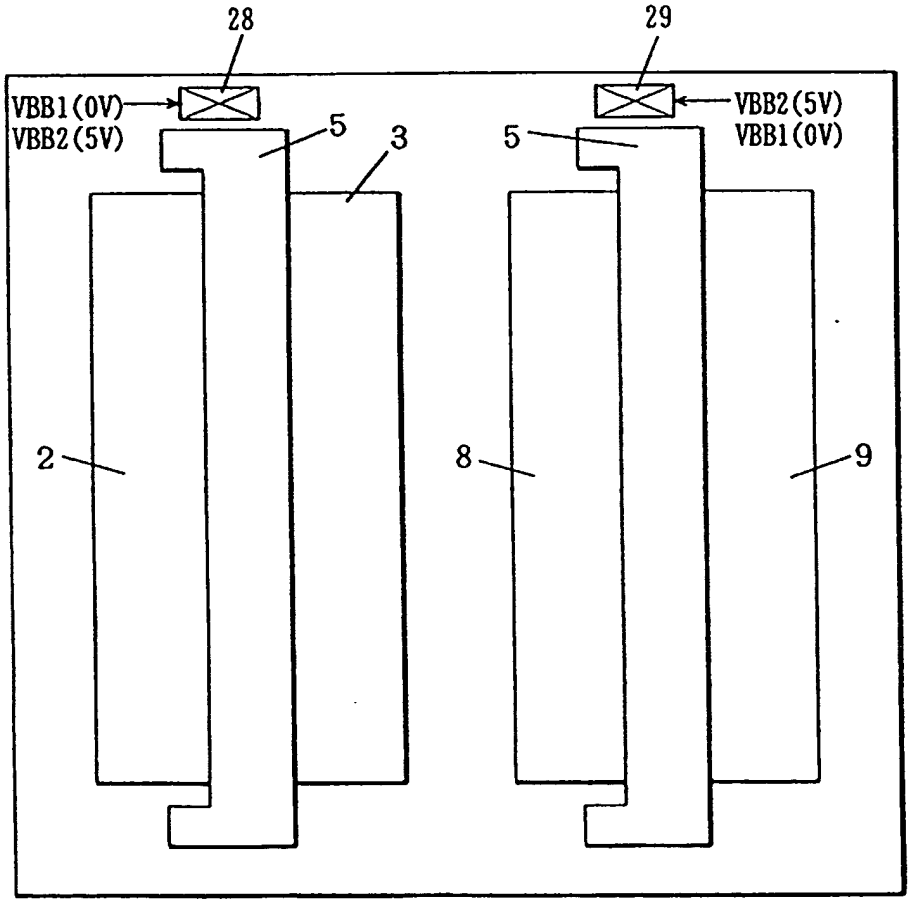
28
29
VBB1(0V)
VBB2(5V)
VBB2(5V)
VBB1(0V)
5
3
5
2
8
9

FIG. 18

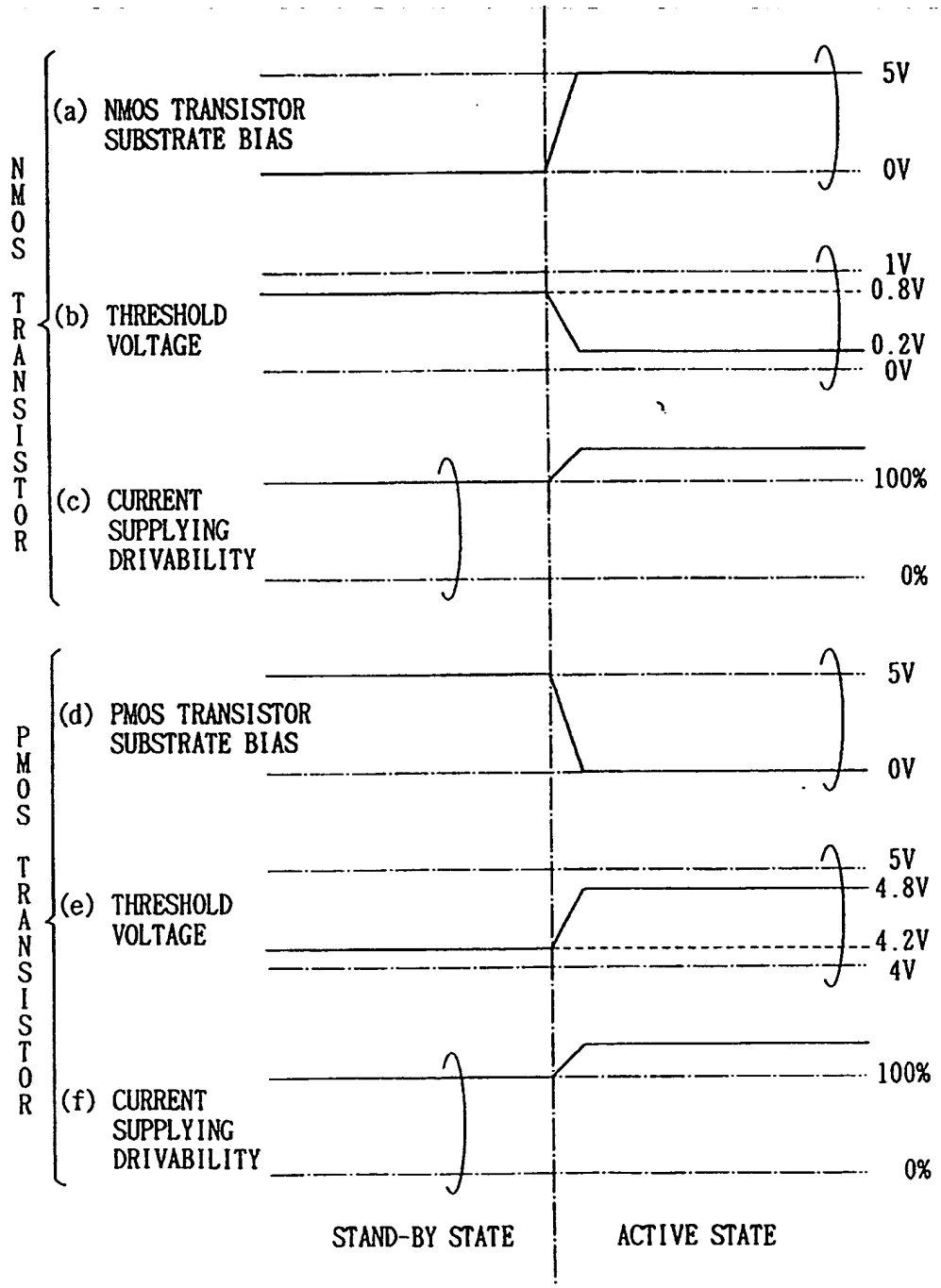
NMOS TRANSISTOR
(a) NMOS TRANSISTOR SUBSTRATE BIAS
5V
0V
(b) THRESHOLD VOLTAGE
1V
0.8V
0.2V
0V
(c) CURRENT SUPPLYING DRIVABILITY
100%
0%
PMOS TRANSISTOR
(d) PMOS TRANSISTOR SUBSTRATE BIAS
5V
0V
(e) THRESHOLD VOLTAGE
5V
4.8V
4.2V
4V
(f) CURRENT SUPPLYING DRIVABILITY
100%
0%
STAND-BY STATE
ACTIVE STATE

FIG. 19

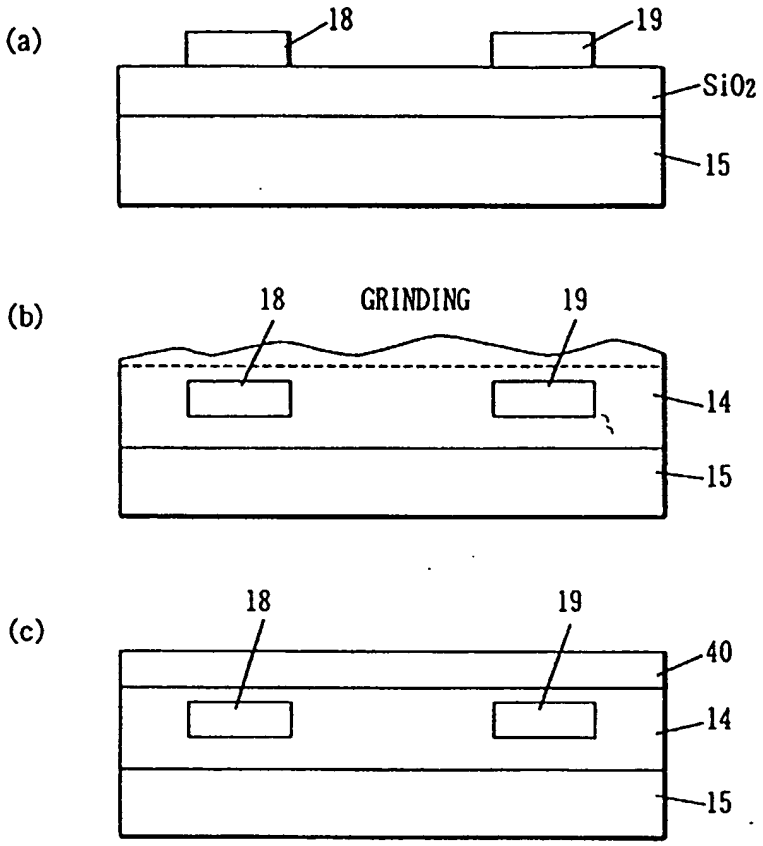

FIG. 20

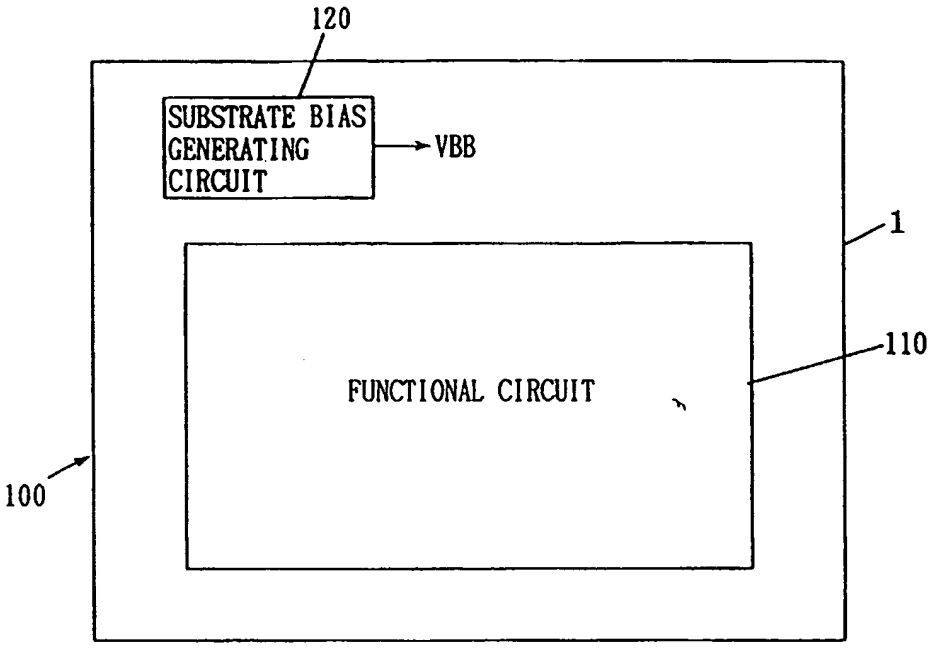
120
SUBSTRATE BIAS GENERATING CIRCUIT
VBB
1
110
FUNCTIONAL CIRCUIT
100

FIG. 21

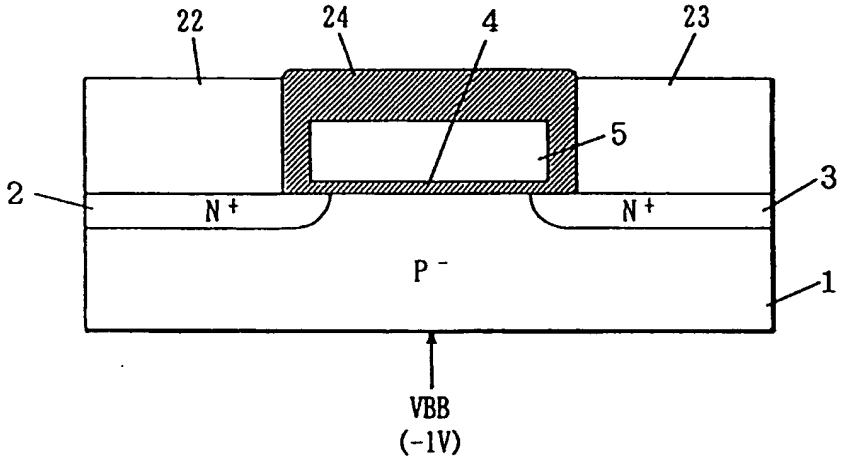
22
24
4
23
5
2
3
N+
N+
P-
1
VBB
(-1V)

FIG. 22

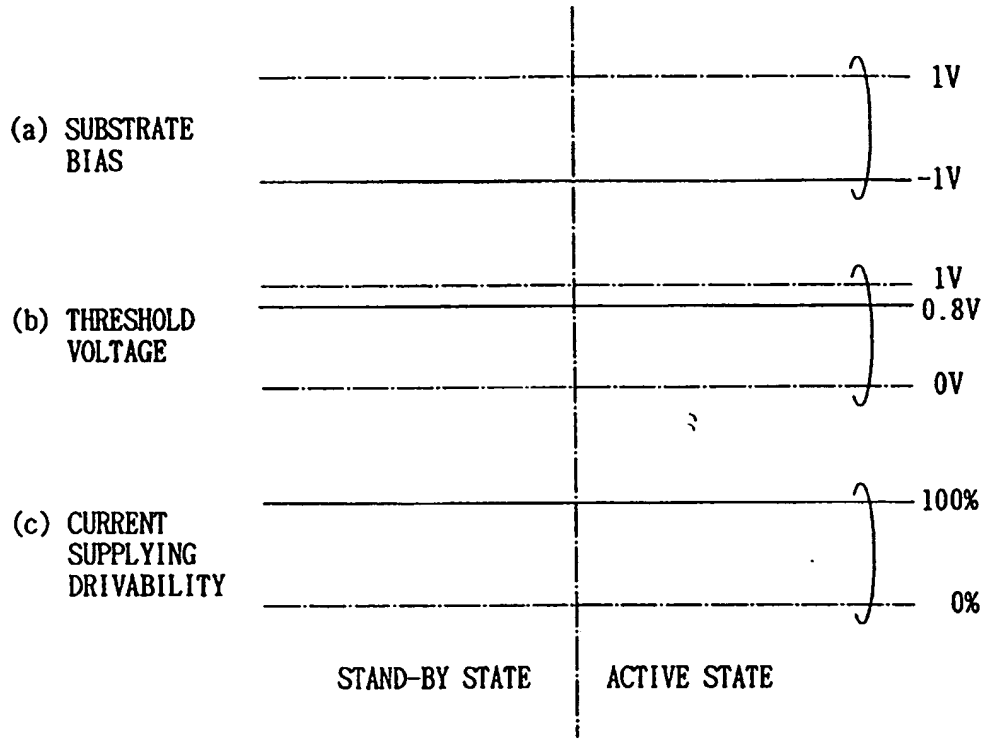
(a) SUBSTRATE BIAS
1V
-1V
(b) THRESHOLD VOLTAGE
1V
0.8V
0V
(c) CURRENT SUPPLYING DRIVABILITY
100%
0%
STAND-BY STATE
ACTIVE STATE

FIG. 23

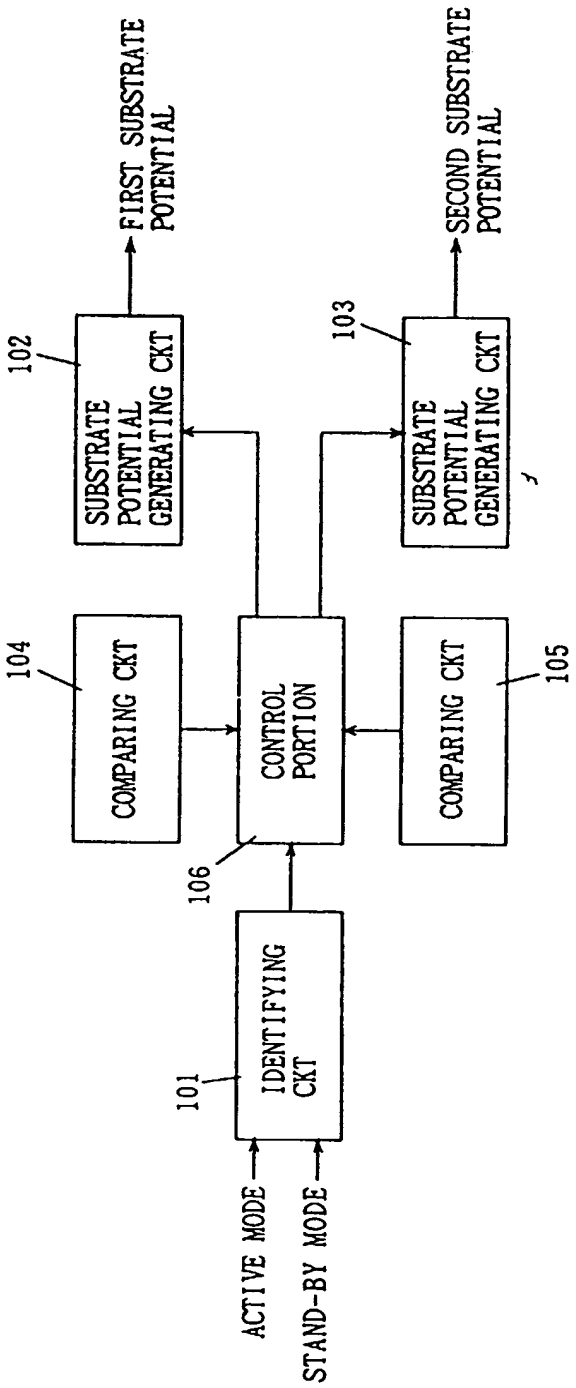
FIRST SUBSTRATE POTENTIAL
SECOND SUBSTRATE POTENTIAL
102
103
SUBSTRATE POTENTIAL GENERATING CKT
SUBSTRATE POTENTIAL GENERATING CKT
104
105
COMPARING CKT
CONTROL PORTION
COMPARING CKT
106
101
IDENTIFYING CKT
ACTIVE MODE
STAND-BY MODE

FIG. 24